FIG. 1

PRIOR ART

OVER THE AIR BROADCAST SPECTRUM

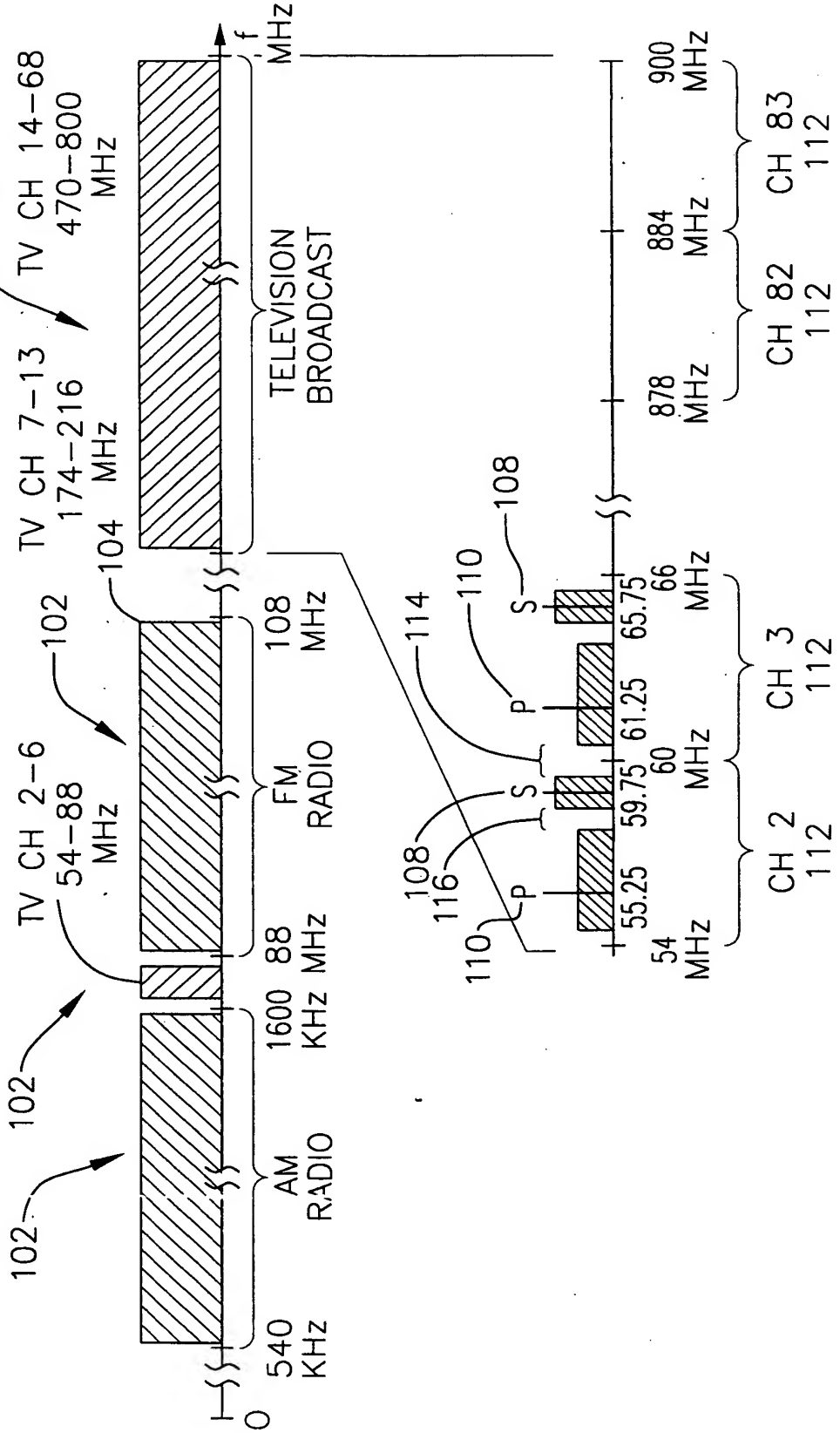


FIG.2

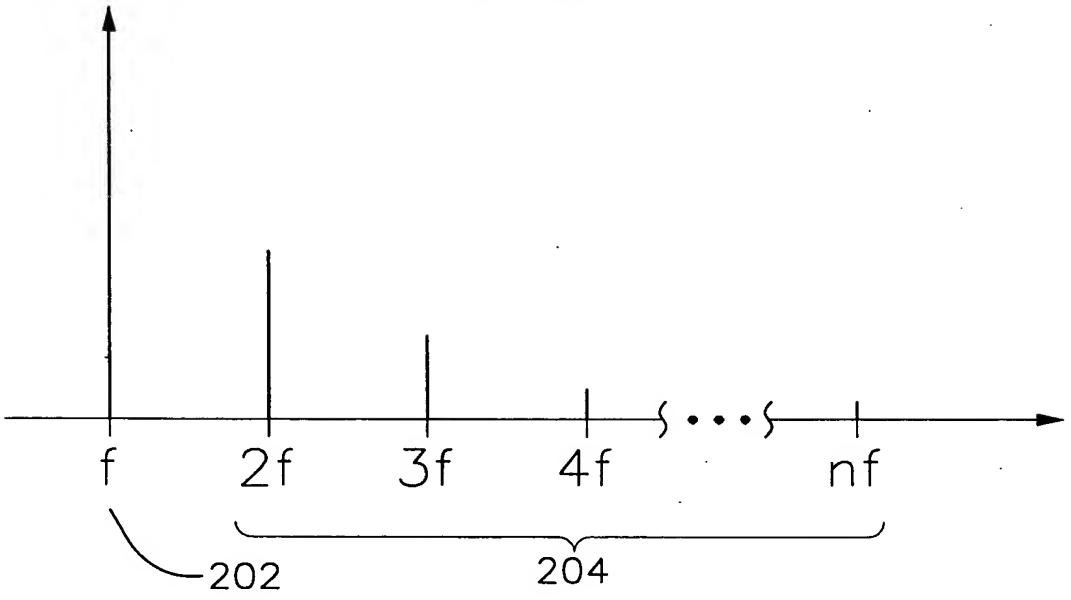
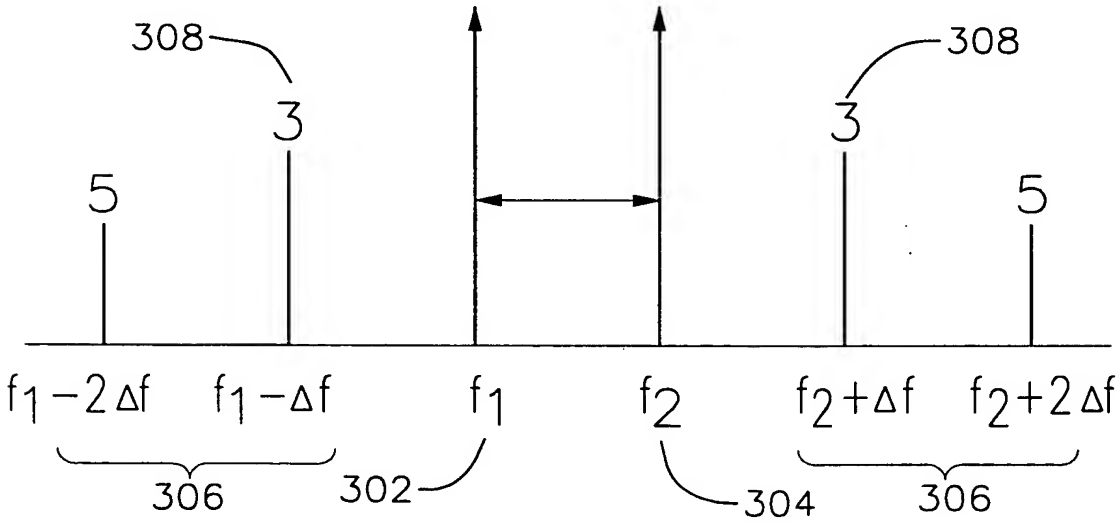


FIG.3
PRIOR ART



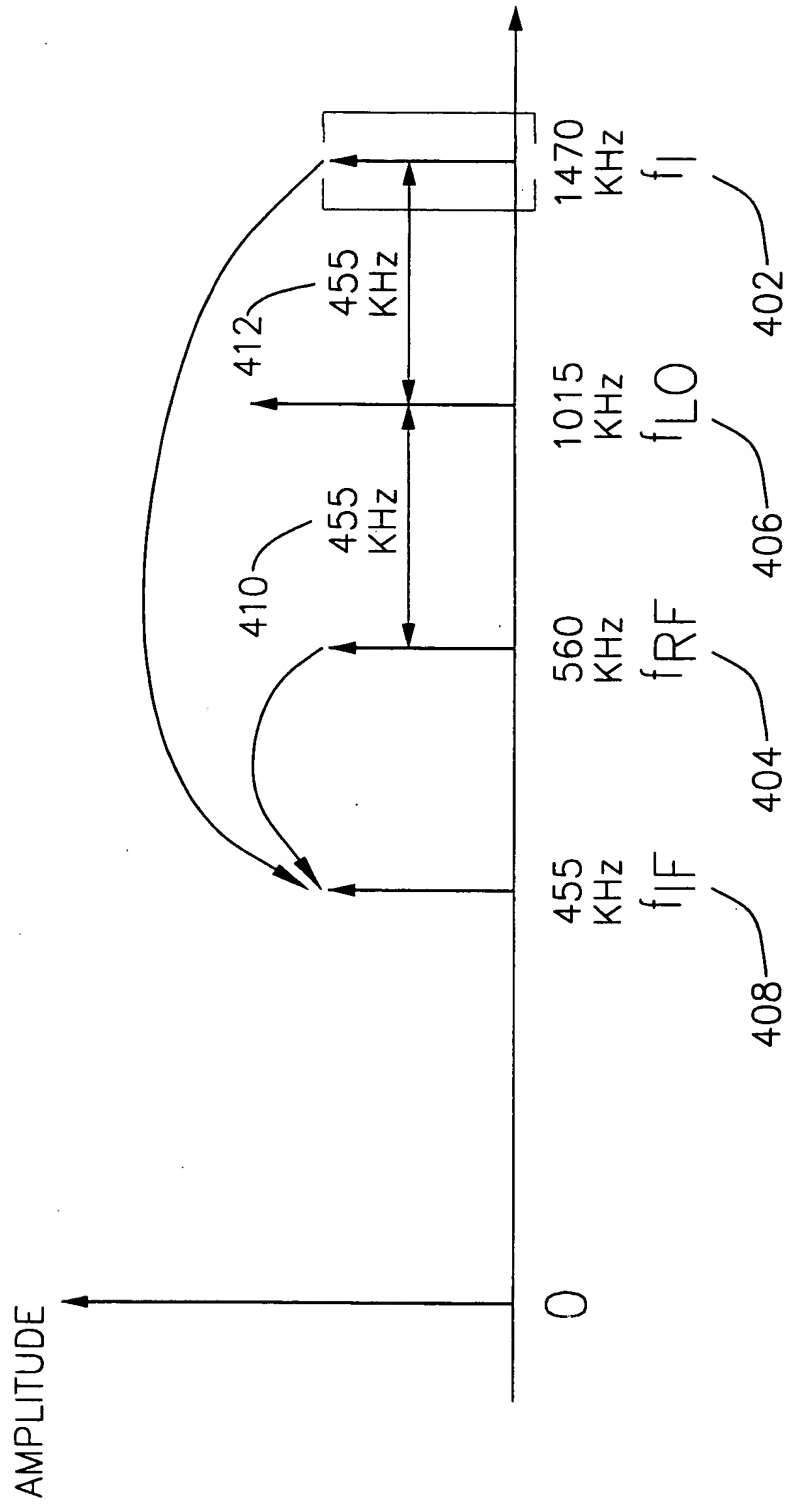


FIG. 4
PRIOR ART

FIG.5

DUAL CONVERSION RECEIVER

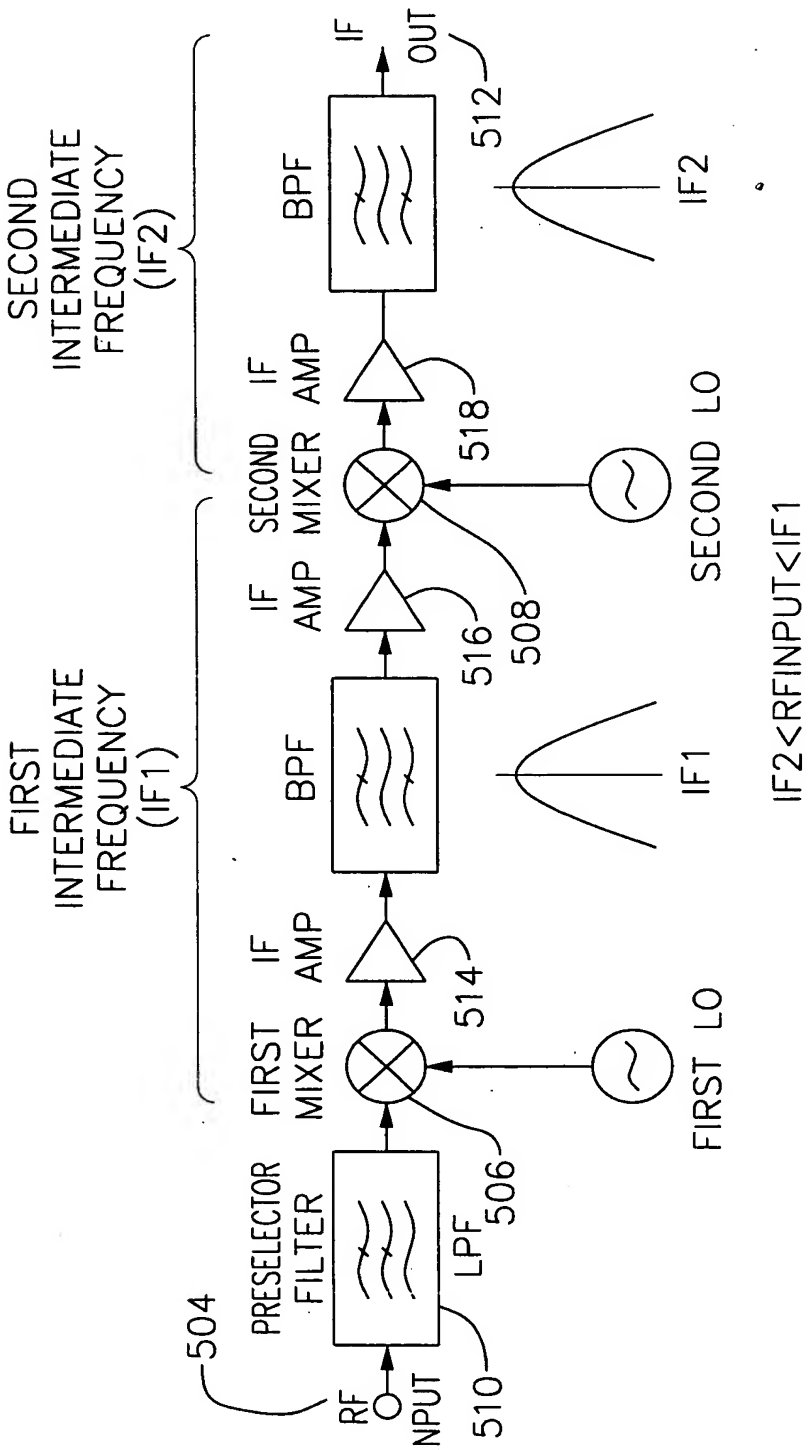


FIG. 6

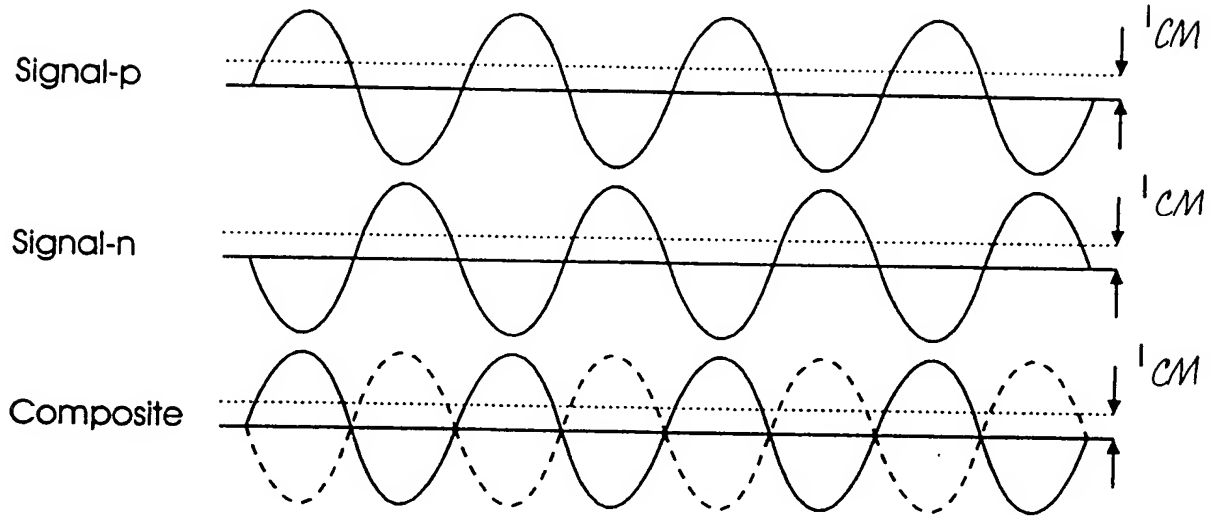

Signal-p
Signal-n
Composite
I_{CM}
I_{CM}
I_{CM}

FIG. 7

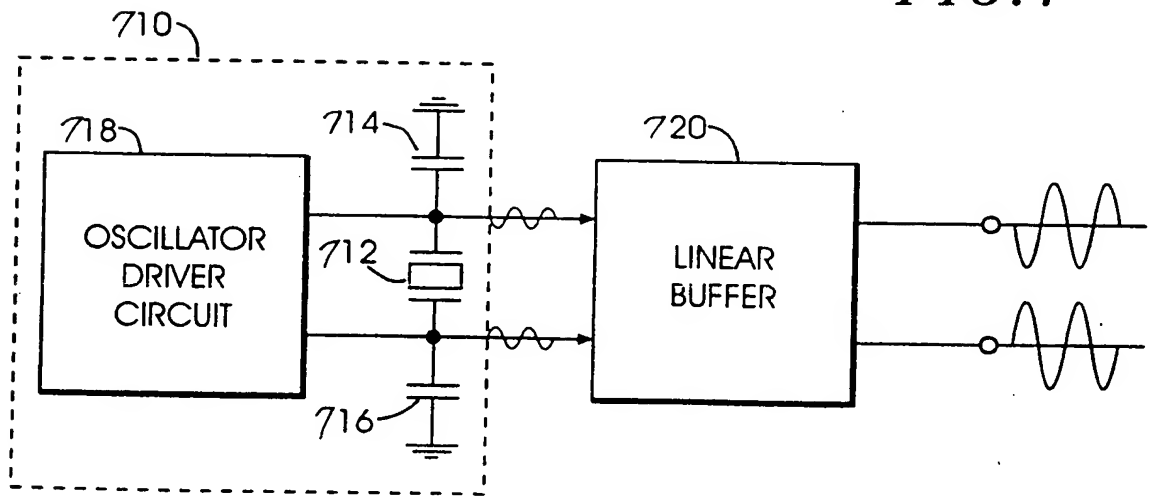

710
718
OSCILLATOR DRIVER CIRCUIT
714
712
716
720
LINEAR BUFFER

FIG. 8

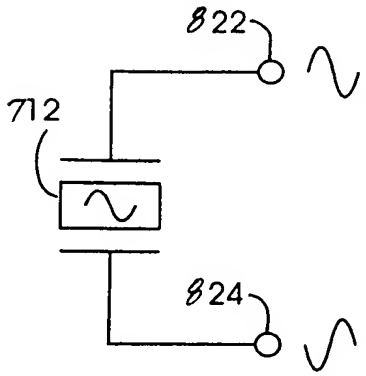


FIG. 9

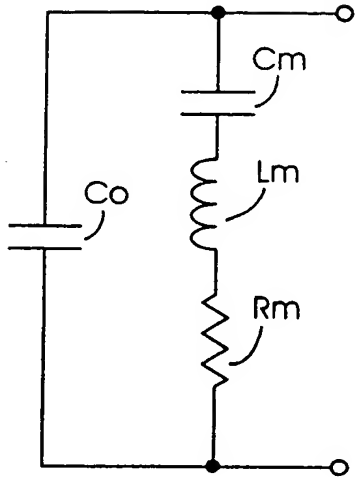


FIG. 10

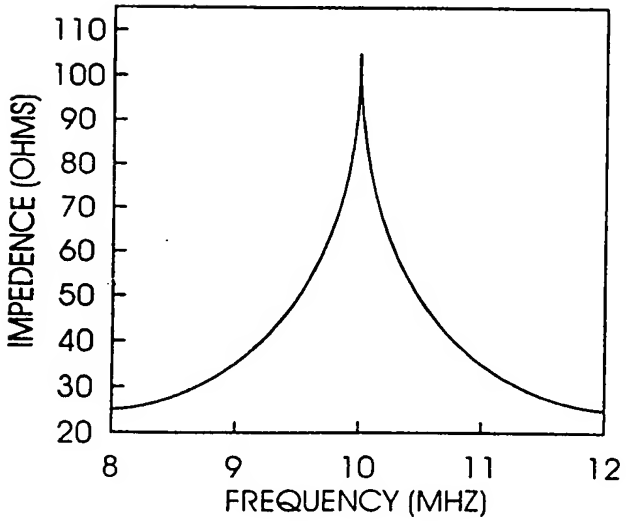


FIG. 11

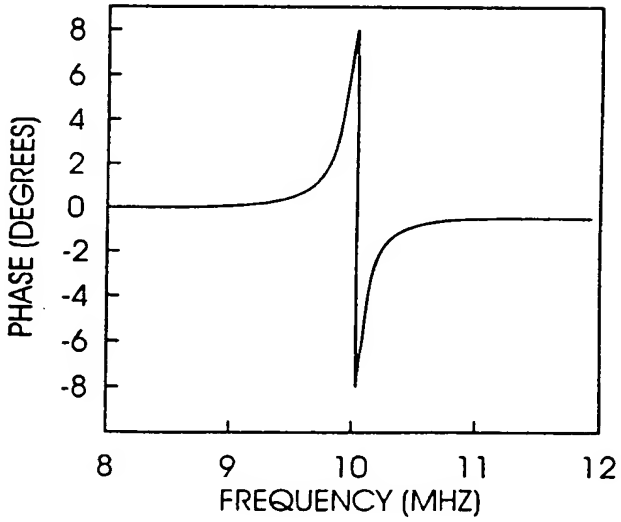


FIG. 12

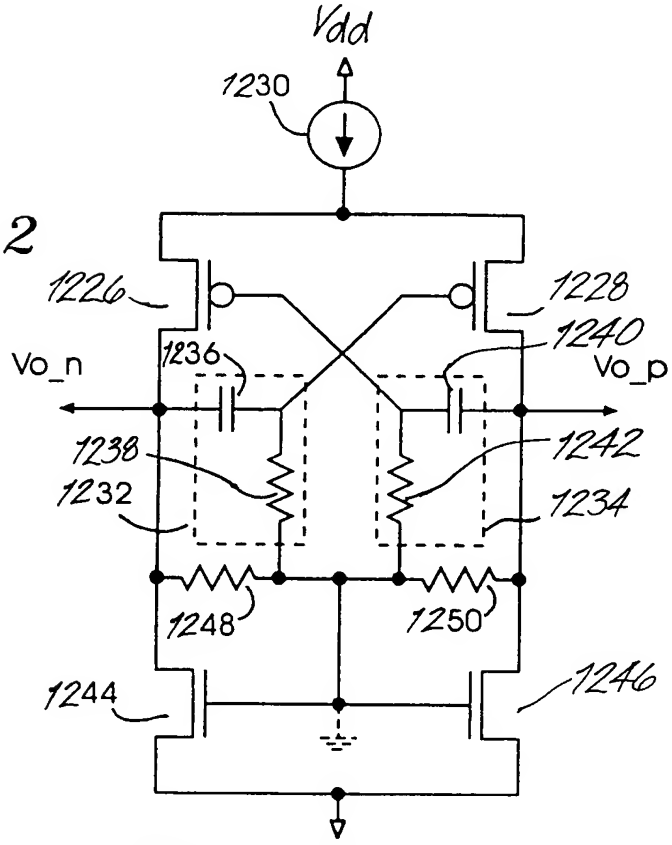

Vdd
1230
1226
1228
1240
Vo_n
1236
Vo_p
1238
1242
1232
1234
1248
1250
1244
1246
Vss

FIG. 13

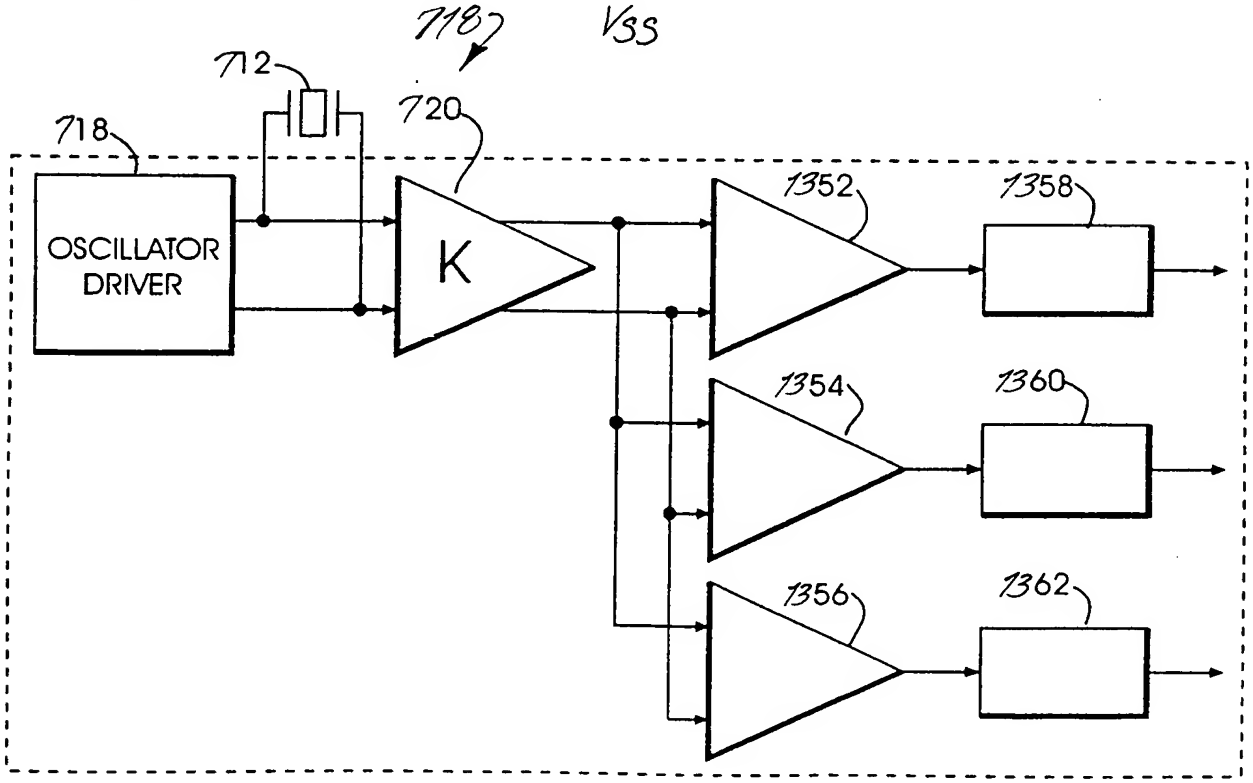
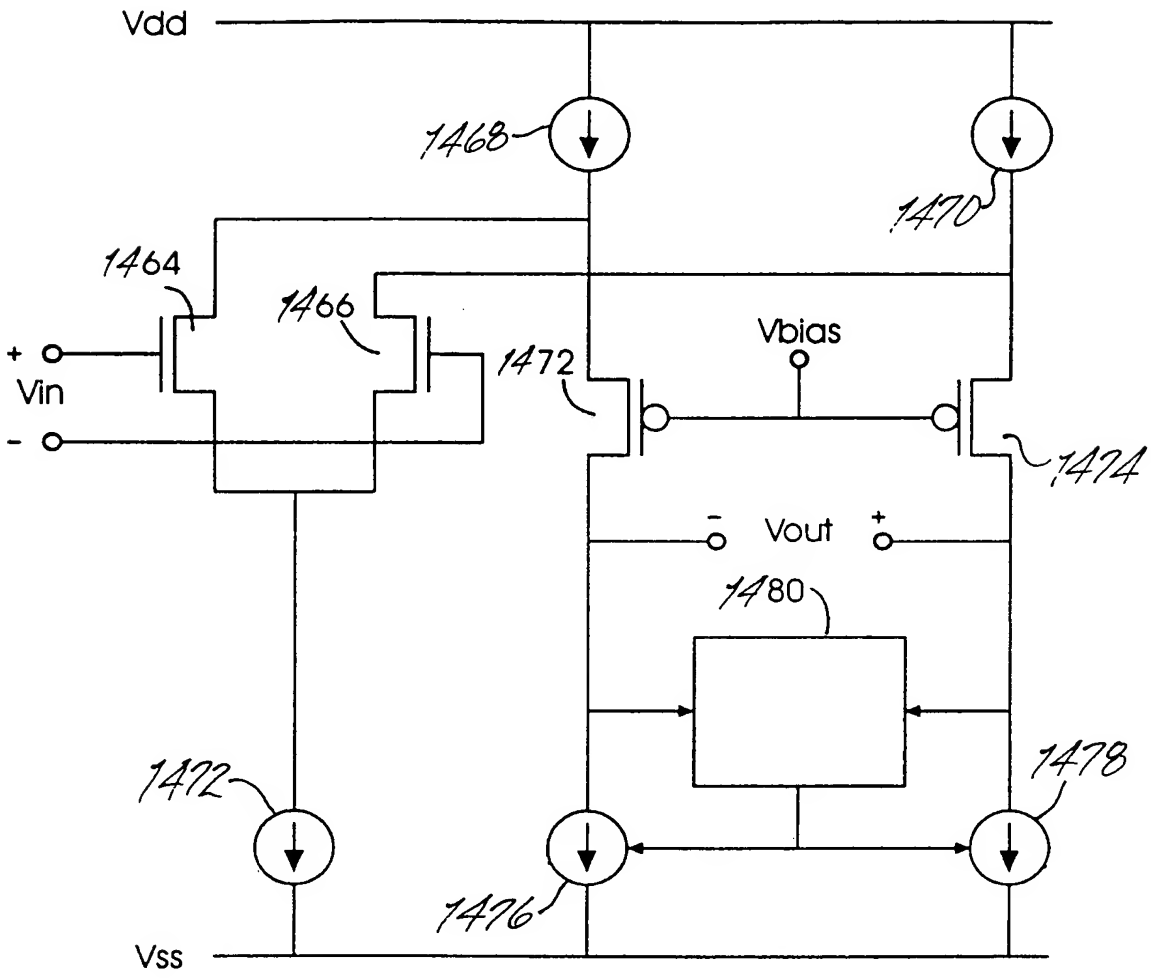

718?
712
720
718
OSCILLATOR DRIVER
K
1352
1358
1354
1360
1356
1362

FIG. 14


Vdd
1468
1470
1464
1466
Vbias
+
Vin
-
1472
1474
-
Vout
+
1480
1472
1478
1476
Vss

Appl. No. To Be Assigned; Filed: Feb 23, 2004
Dkt No. 1875.095000I/JTH/TAD; Group Unit: To Be Assigned
Inventors: Ward, et al Tel: 202-371-2600
Title: Applications for Differential Crystal Oscillator (as amended)

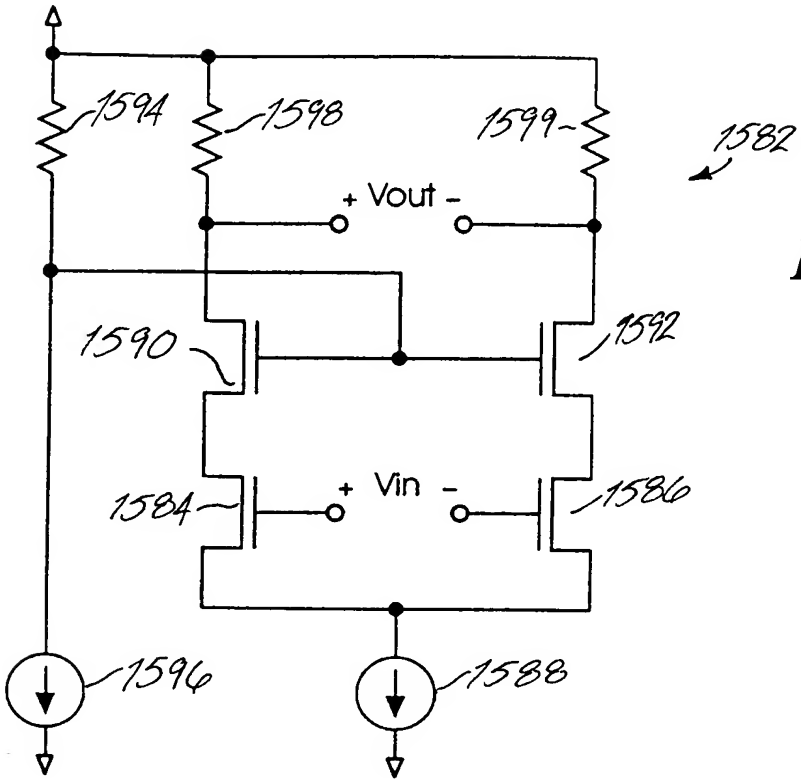


FIG. 15

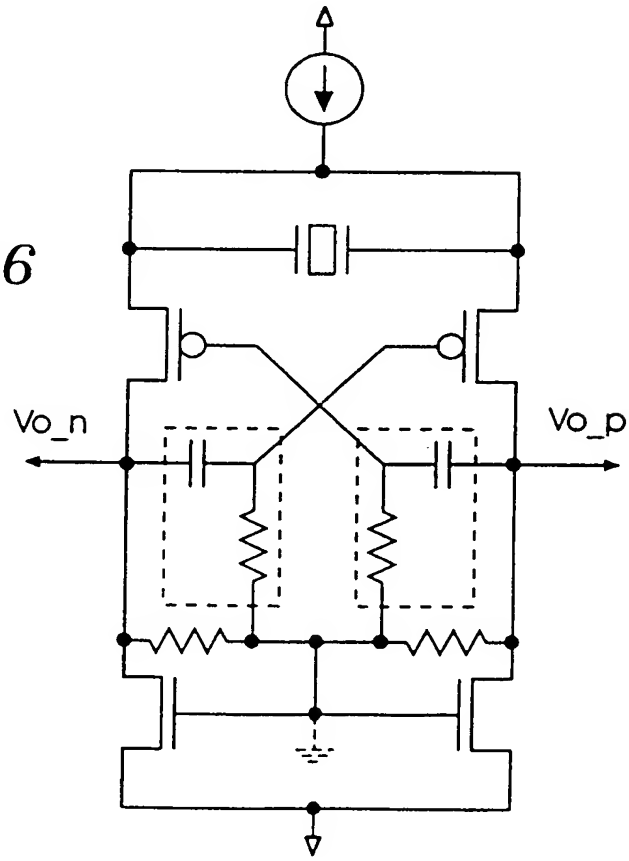


FIG. 16

FIG. 17

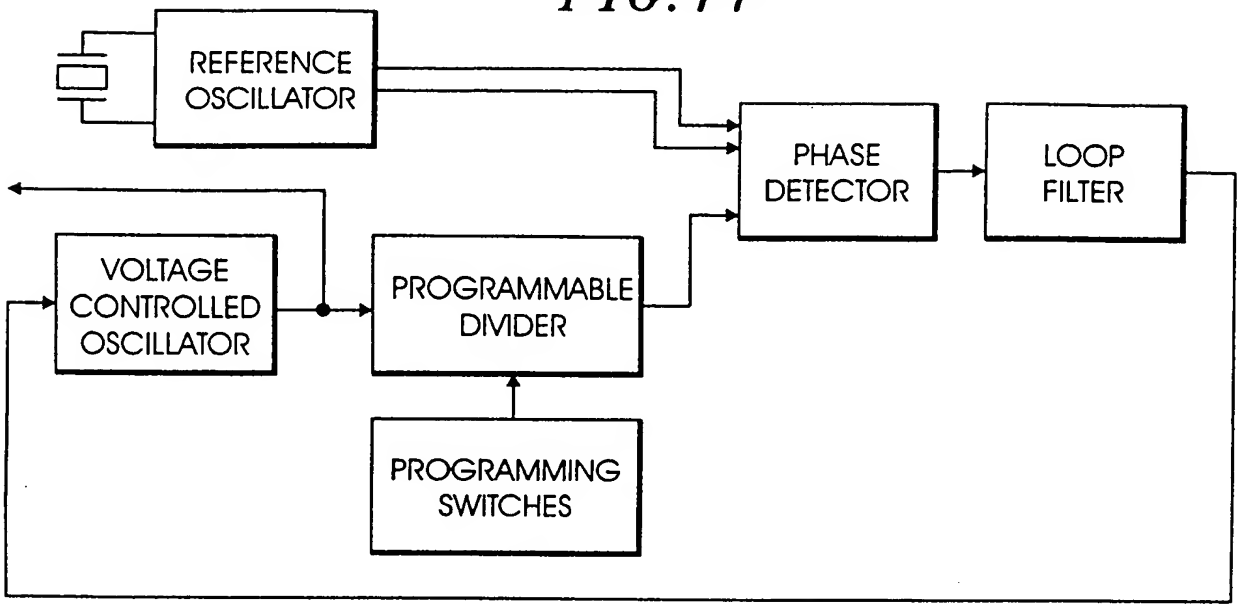

REFERENCE OSCILLATOR
PHASE DETECTOR
LOOP FILTER
VOLTAGE CONTROLLED OSCILLATOR
PROGRAMMABLE DIVIDER
PROGRAMMING SWITCHES

FIG. 18

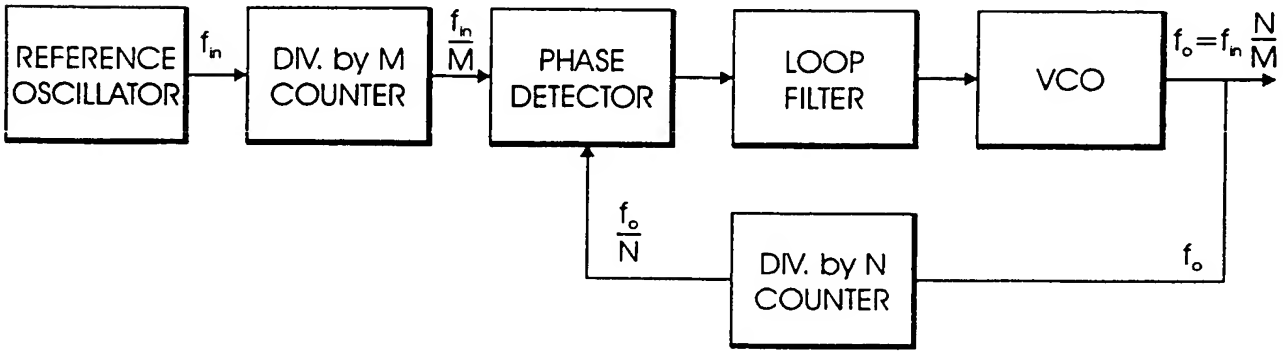

REFERENCE OSCILLATOR
f_{in}
DIV. by M COUNTER
$\frac{f_{in}}{M}$
PHASE DETECTOR
LOOP FILTER
VCO
$f_o = f_{in} \frac{N}{M}$
$\frac{f_o}{N}$
DIV. by N COUNTER
f_o

FIG. 19

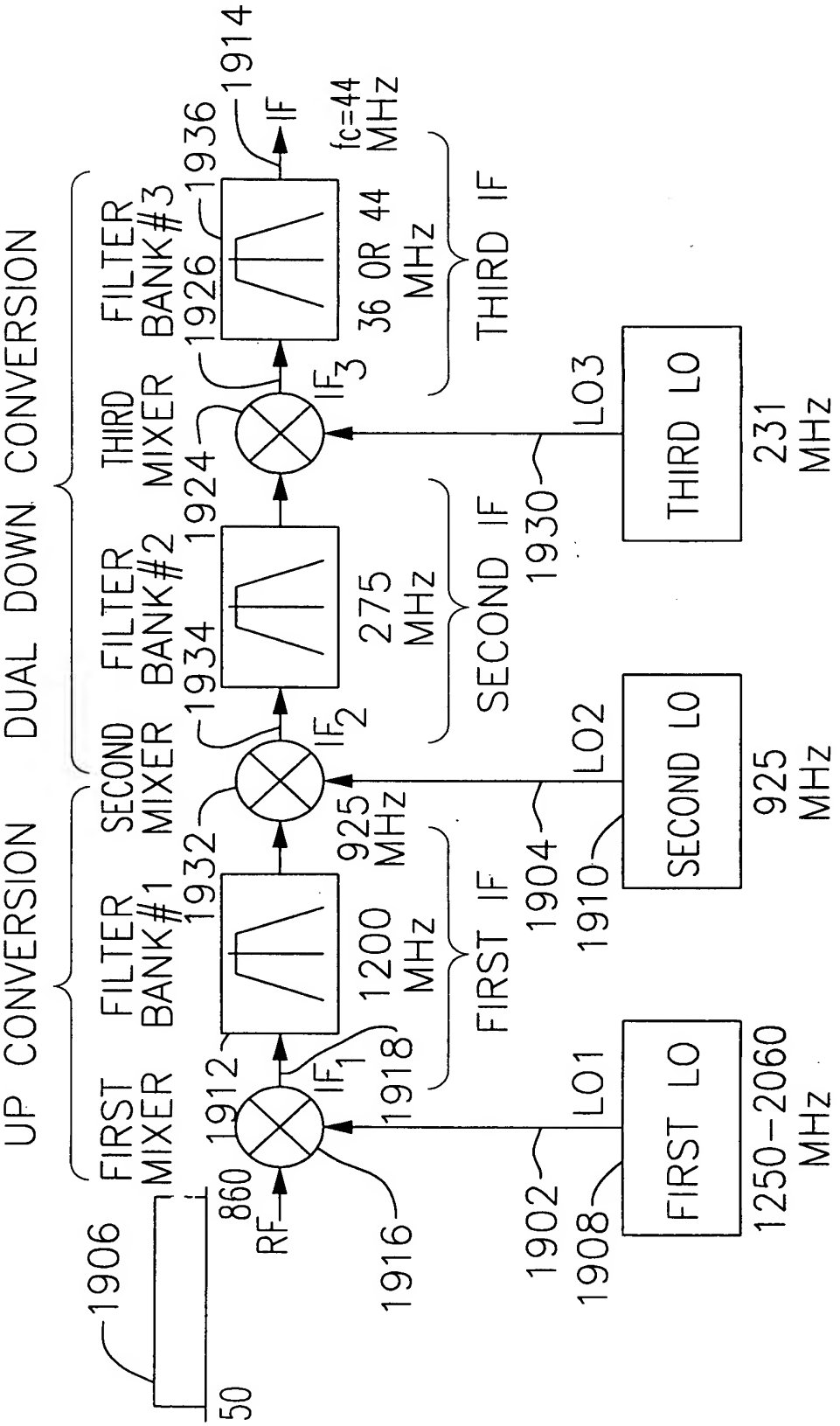

UP CONVERSION
DUAL DOWN CONVERSION
1906
50
FIRST MIXER
1912
860
RF
1916
FILTER BANK#1
1932
IF1
1200 MHz
1918
SECOND MIXER
1934
925 MHz
IF2
FILTER BANK#2
1924
275 MHz
THIRD MIXER
1926
IF3
FILTER BANK#3
1936
1914
IF
fc=44 MHz
36 OR 44 MHz
THIRD IF
FIRST IF
SECOND IF
1902
1908
FIRST LO
LO1
1250-2060 MHz
1904
1910
SECOND LO
LO2
925 MHz
1930
THIRD LO
LO3
231 MHz

FIG.20

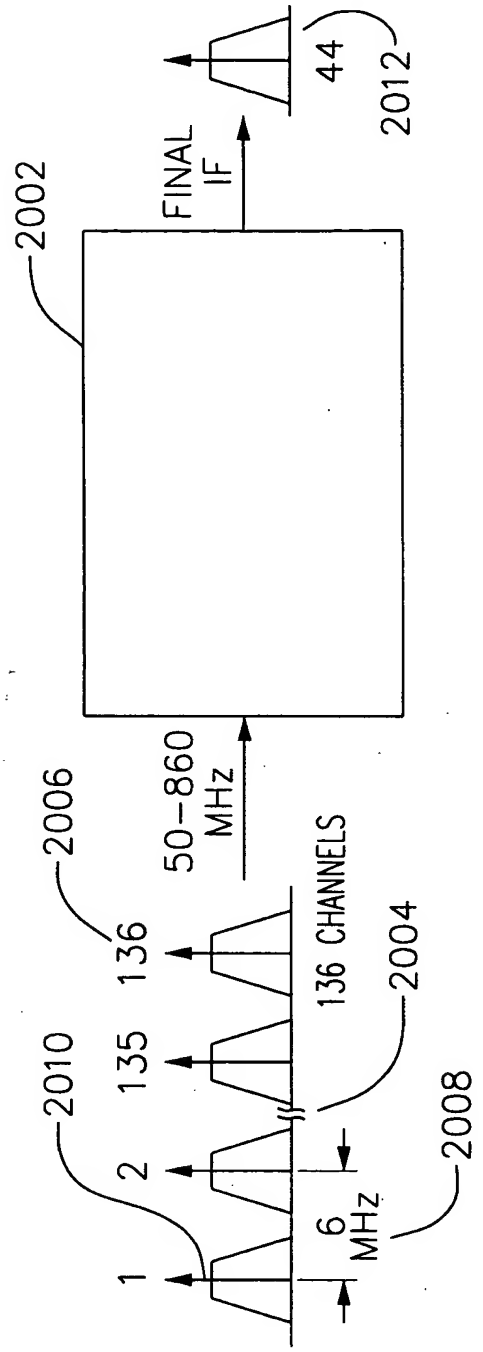

2002
FINAL IF
44
2012
50–860 MHz
2006
136
135
2
1
2010
136 CHANNELS
2004
6 MHz
2008

FIG. 21

PPL Xtal REFERENCE=10MHz
LO-1, 10MHz FREQUENCY STEPS
LO-2, 100kHz FREQUENCY STEPS

44MHz IF

TABLE OF FREQUENCIES BASED ON COARSE/FINE PLL SOLUTION:

NOTE
- LO-2 REF=100KHz, SO DIVIDE RANGE=9216 TO 9280

Frf (MHz)	50	56	62	68	74	80	86	92	98	104	110	116	122	128	"	854	860
LO-1(MHz)	1250	1260	1260	1270	1270	1280	1290	1290	1300	1300	1310	1320	1320	1330	"	2050	2060
IF-1 (MHz)	**1200**	1204	1198	1202	1196	**1200**	1204	1198	1202	1196	**1200**	1204	1198	1202	"	1196	**1200**
LO-2(MHz)	**924.8**	928.0	923.2	926.4	921.6	**924.8**	928.0	923.2	926.4	921.6	**924.8**	928.0	923.2	926.4	"	921.6	**924.8**
IF-2(MHz)	**275.2**	276.0	274.8	275.6	274.4	**275.2**	276.0	274.8	275.6	274.4	**275.2**	276.0	274.8	275.6	"	274.4	**275.2**
LO-3(MHz)	231.2	232	230.8	232	230	231	232	231	232	230	231	232	231	232	"	230	231
IF-3(MHz)	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	"	44.0	44.0

2102

Sheet 13 of 50
Appl. No. To Be Assigned; Filed: Feb 23, 2004
Dkt No. 1875.095000/JTH/TAD; Group Unit: To Be Assigned
Inventors: Ward, et al Tel: 202-371-2600
Title: Applications for Differential Crystal Oscillator (as amended)

FIG.22

PPL Xtal REFERENCE=10MHz
LO-1, 10MHz FREQUENCY STEPS
LO-2, 100kHz FREQUENCY STEPS

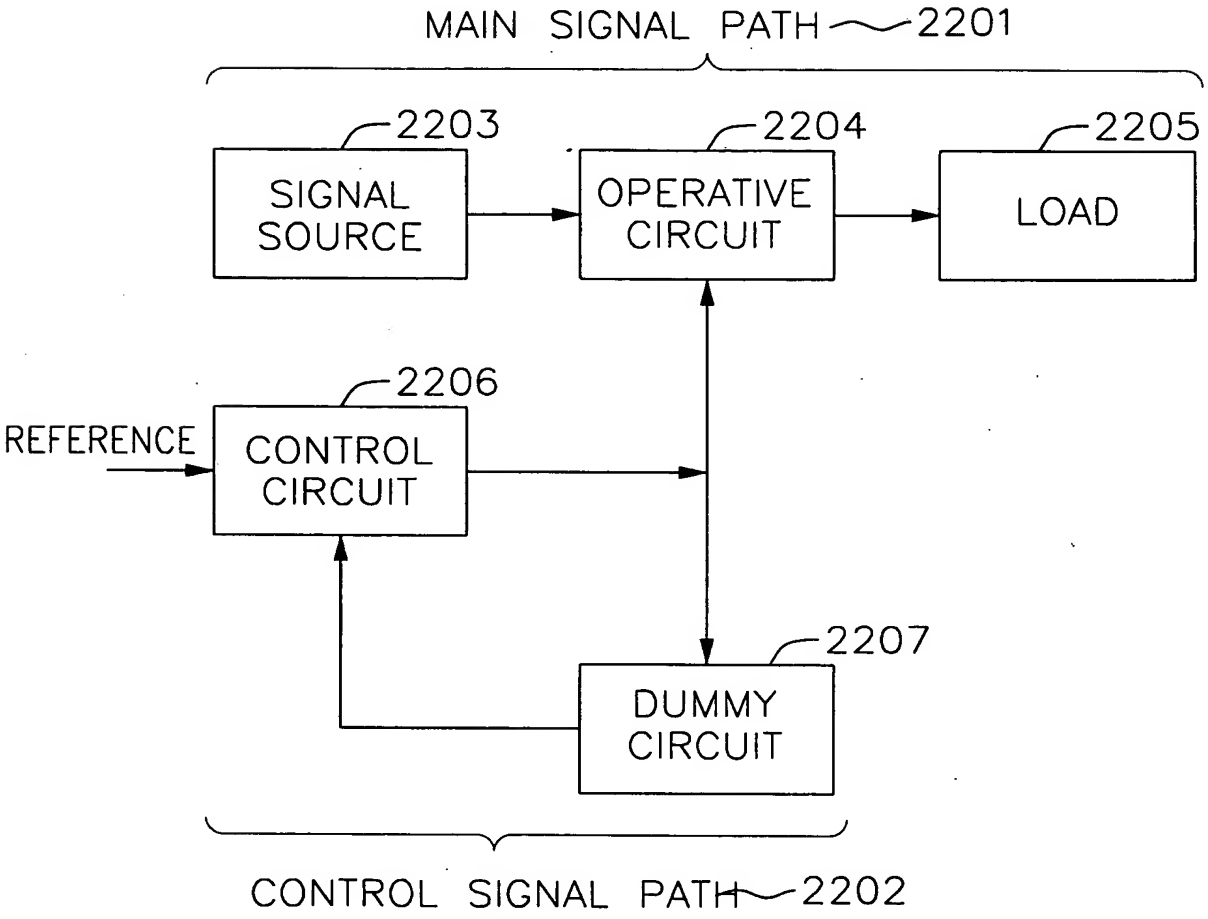
36MHz IF

TABLE OF FREQUENCIES BASED ON COARSE/FINE PLL SOLUTION:

NOTE
- LO-2 REF=100KHz, SO DIVIDE RANGE=9280 TO 9340

Frf (MHz)	50	58	66	74	82	90	98	106	114	122	130	138	146	154	"	852	860
LO-1(MHz)	1250	1260	1270	1270	1280	1290	1300	1310	1310	1320	1330	1340	1350	1350	"	2050	2060
IF-1 (MHz)	**1200**	1202	1204	1196	1198	**1200**	1202	1204	1196	1198	**1200**	1202	1204	1196	"	1198	**1200**
LO-2(MHz)	**931.2**	**932.8**	**934.4**	**928.0**	**930**	**931**	**933**	**934**	**928.0**	**930**	**931**	**933**	**934**	**928.0**	"	**929.60**	**931.2**
IF-2(MHz)	**268.8**	269.2	269.6	268.0	268.4	**268.8**	269.2	269.6	268.0	268.4	**268.8**	269.2	269.6	268.0	"	268.4	**268.8**
LO-3(MHz)	232.8	233.2	233.6	232	232	233	233	234	232	232	233	233	234	232.0	"	232.4	232.8
IF-3(MHz)	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	"	36.0	36.0

FIG.23


MAIN SIGNAL PATH
2201
2203
2204
2205
SIGNAL SOURCE
OPERATIVE CIRCUIT
LOAD
2206
REFERENCE
CONTROL CIRCUIT
2207
DUMMY CIRCUIT
CONTROL SIGNAL PATH
2202

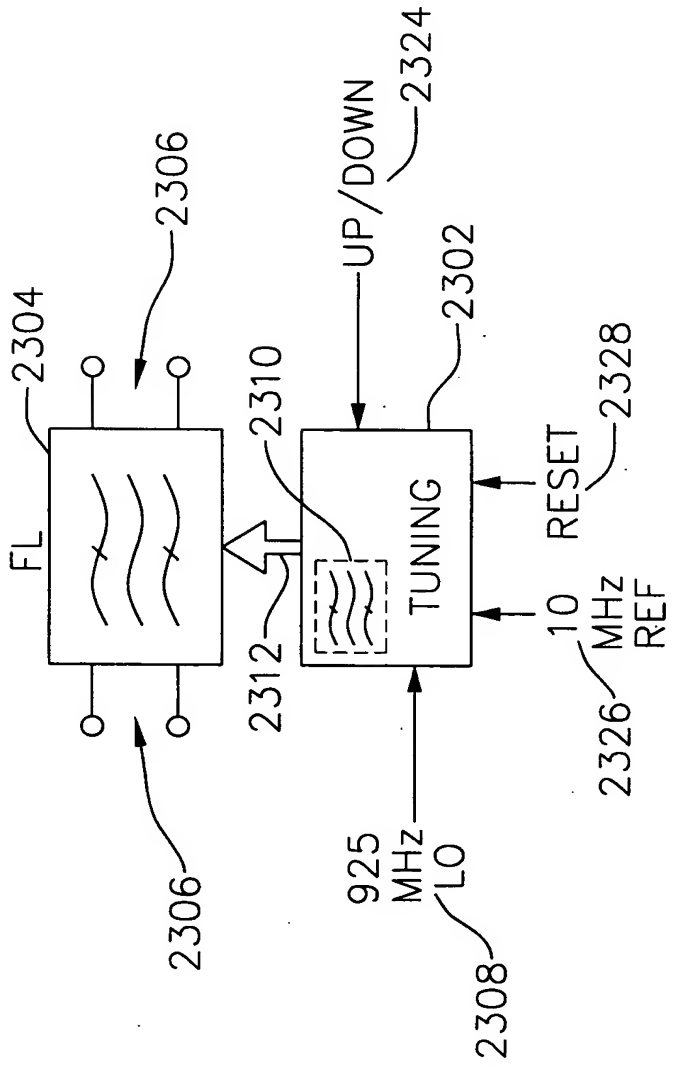
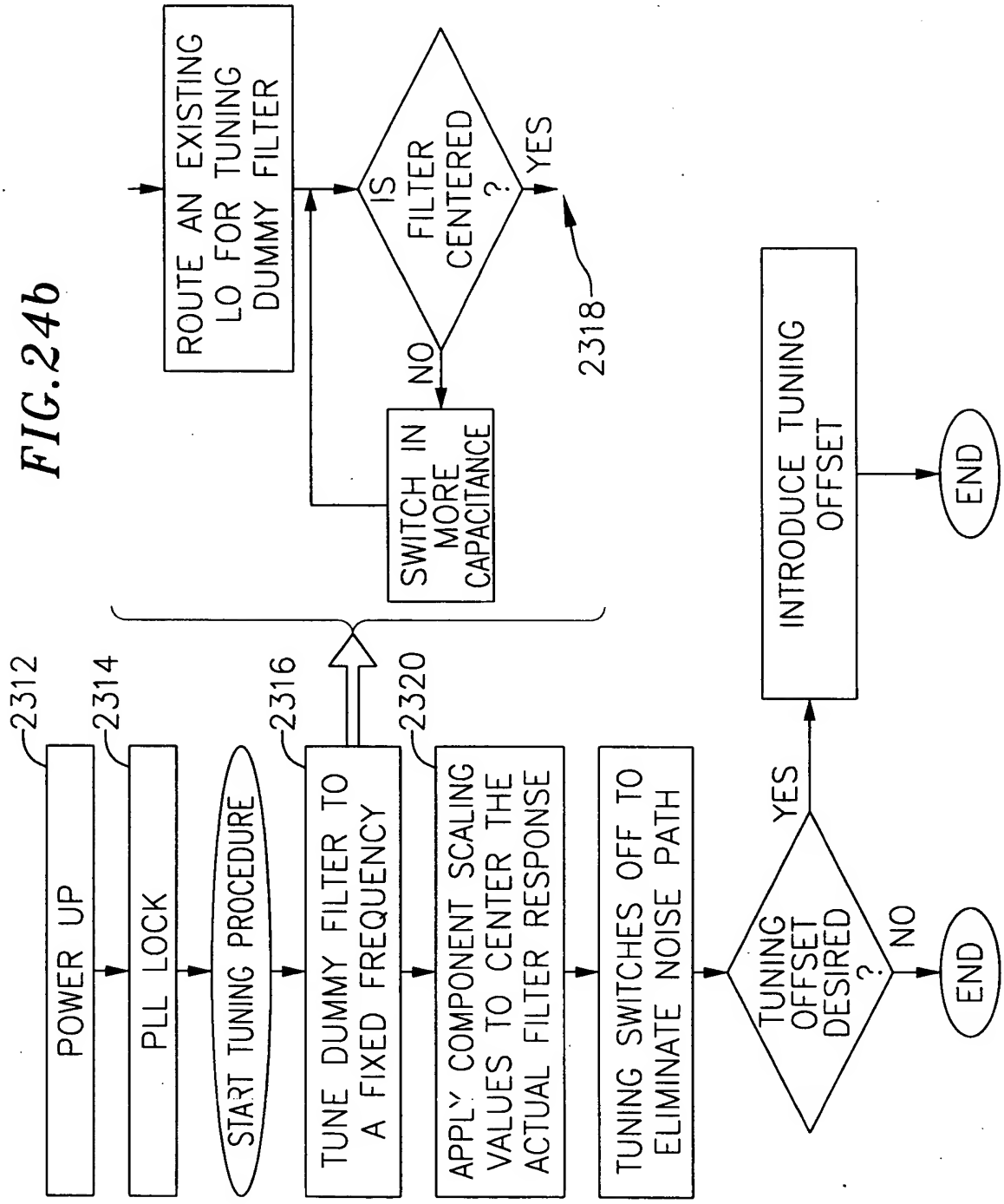

2304
2306
2310
UP/DOWN
2324
2302
2328
FL
TUNING
RESET
10 MHz REF
2312
2326
2306
925 MHz LO
2308

FIG.24a

FIG.24b


POWER UP
2312
PLL LOCK
2314
START TUNING PROCEDURE
2316
TUNE DUMMY FILTER TO A FIXED FREQUENCY
2320
APPLY COMPONENT SCALING VALUES TO CENTER THE ACTUAL FILTER RESPONSE
TUNING SWITCHES OFF TO ELIMINATE NOISE PATH
TUNING OFFSET DESIRED ?
YES
NO
END
INTRODUCE TUNING OFFSET
END
ROUTE AN EXISTING LO FOR TUNING DUMMY FILTER
IS FILTER CENTERED ?
YES
2318
NO
SWITCH IN MORE CAPACITANCE

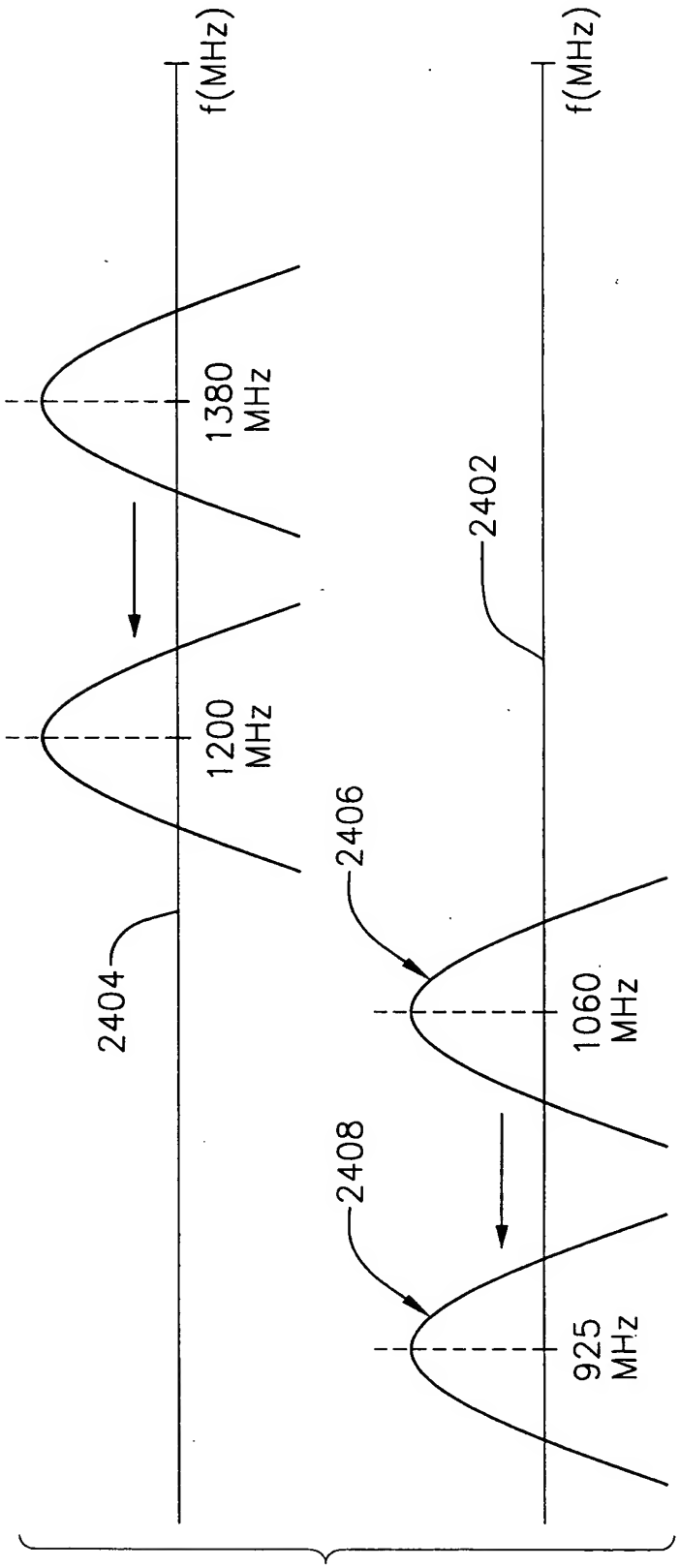

f(MHz)
1380 MHz
1200 MHz
2404
f(MHz)
2402
2406
1060 MHz
2408
925 MHz

FIG.24c

FIG.25

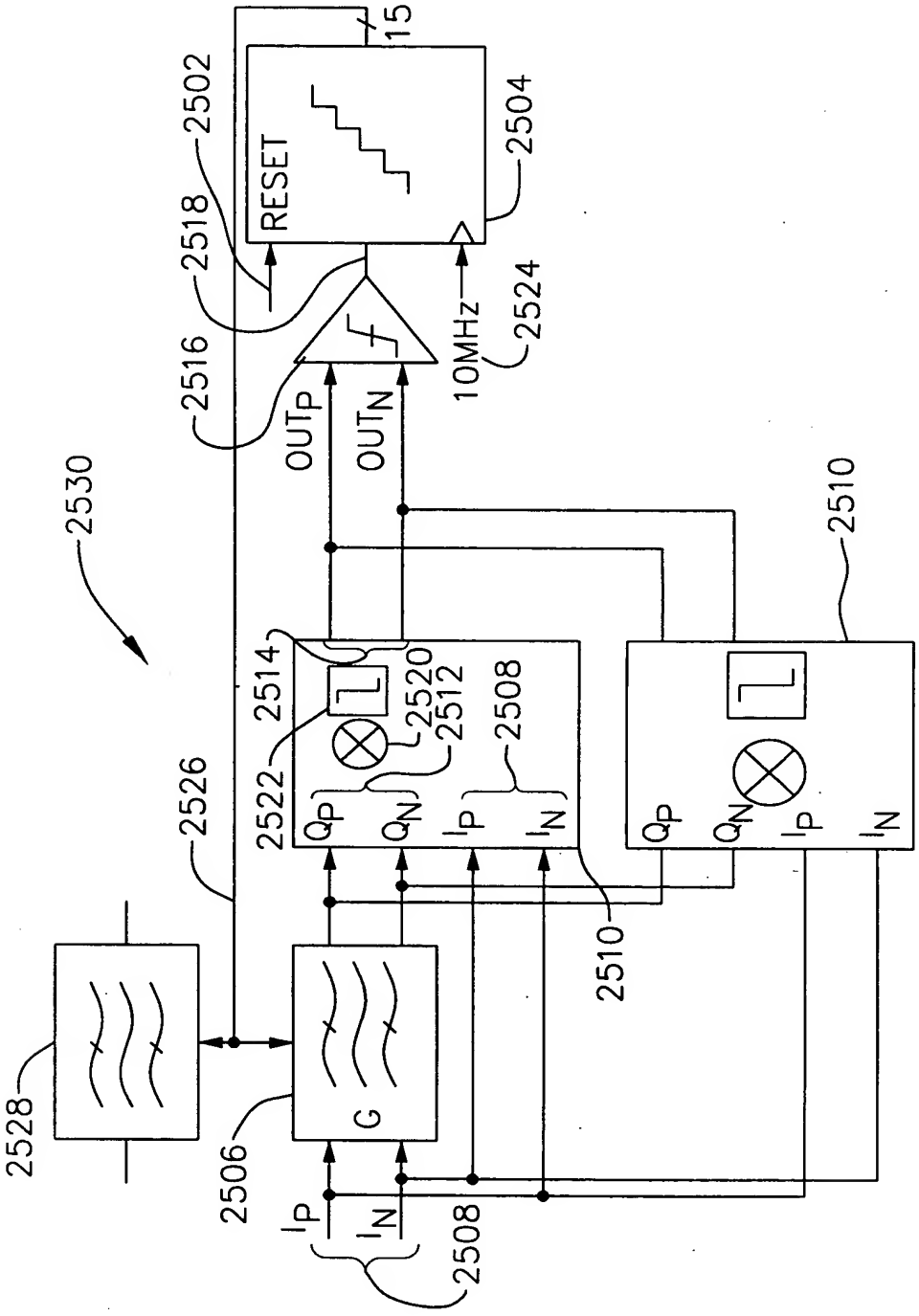
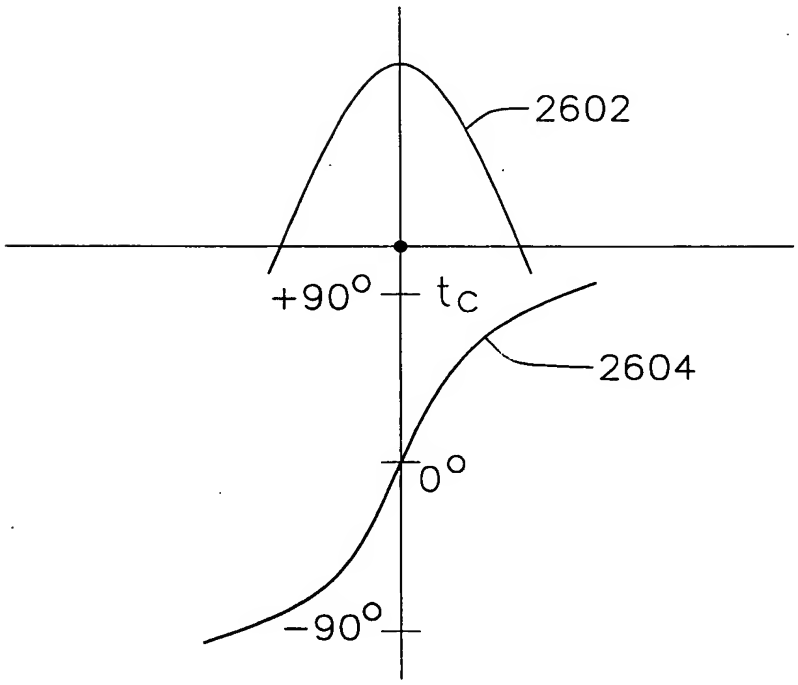

15
2502
2504
RESET
2518
2516
2524
10MHz
OUTP
OUTN
2530
2510
2514
2520
2512
2508
2522
2526
QP
QN
IP
IN
2528
2506
G
2508

FIG.26



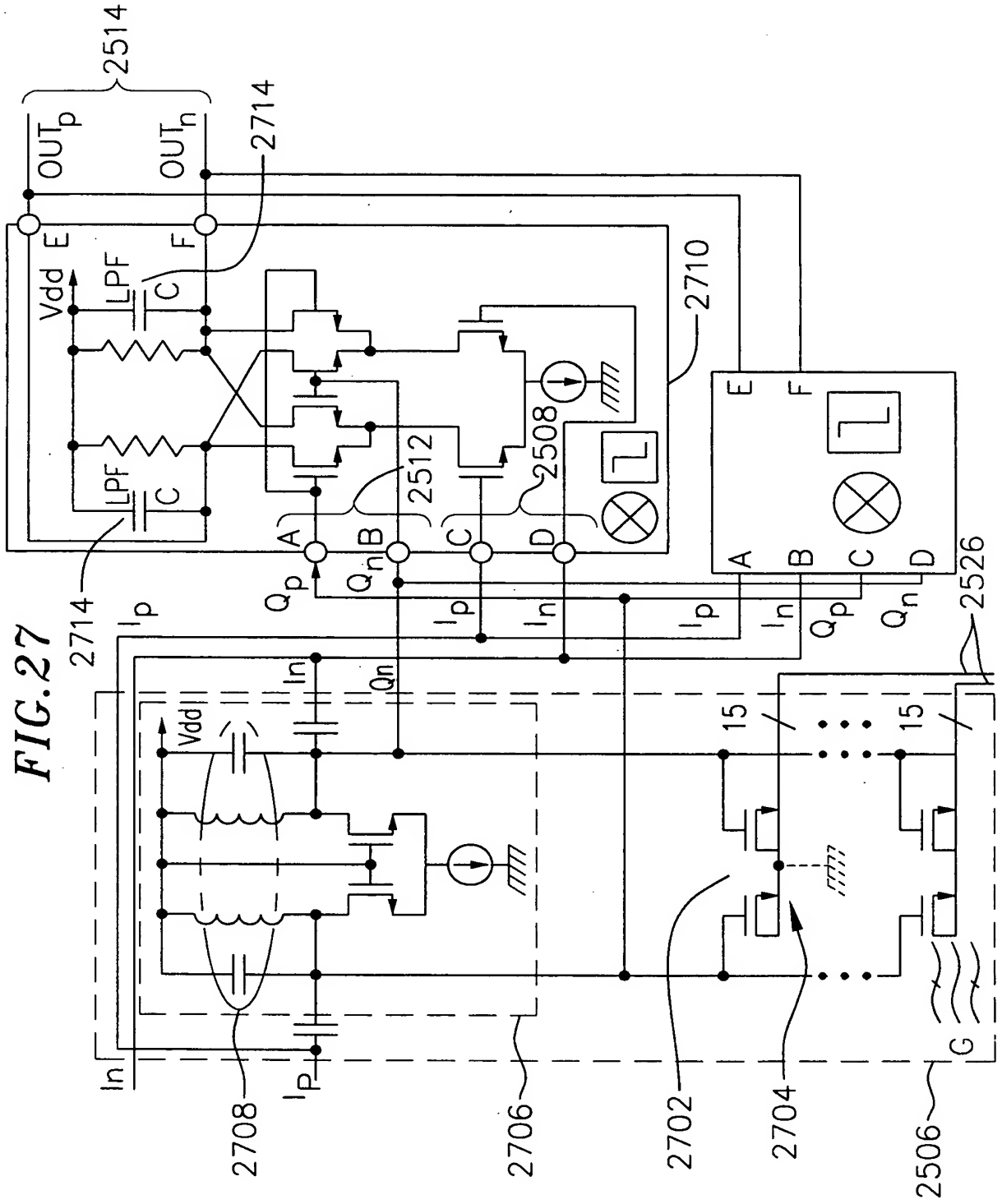

2514
OUTp
OUTn
2714
Vdd
E
F
LPF
C
2710
2512
2508
A
B
C
D
Qp
Qn
Ip
In
2526
15
G
2708
2706
2702
2704
2506

FIG.27

FIG.28

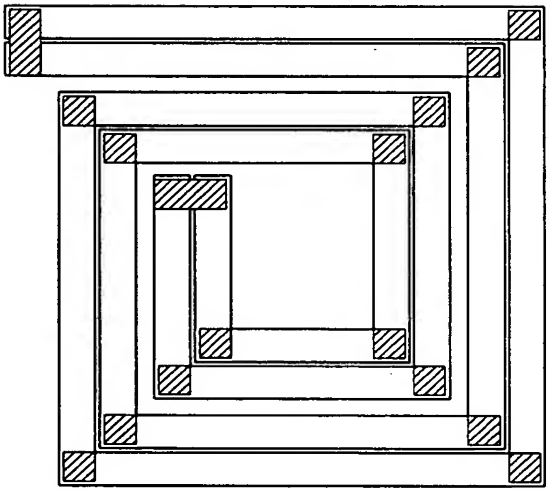


FIG.29

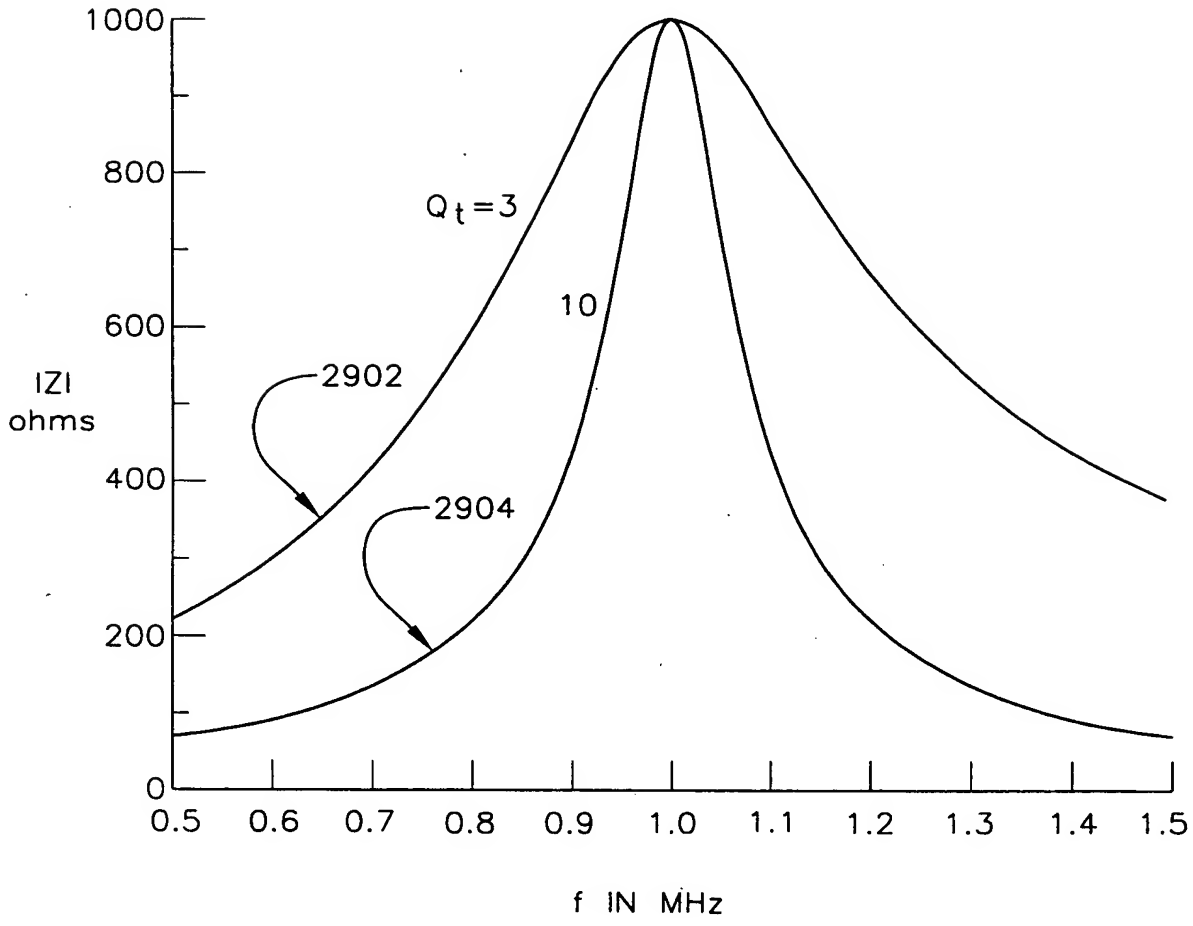

1000
800
600
400
200
0
IZI
ohms
$Q_t = 3$
10
2902
2904
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
1.3
1.4
1.5
f IN MHz

FIG.30

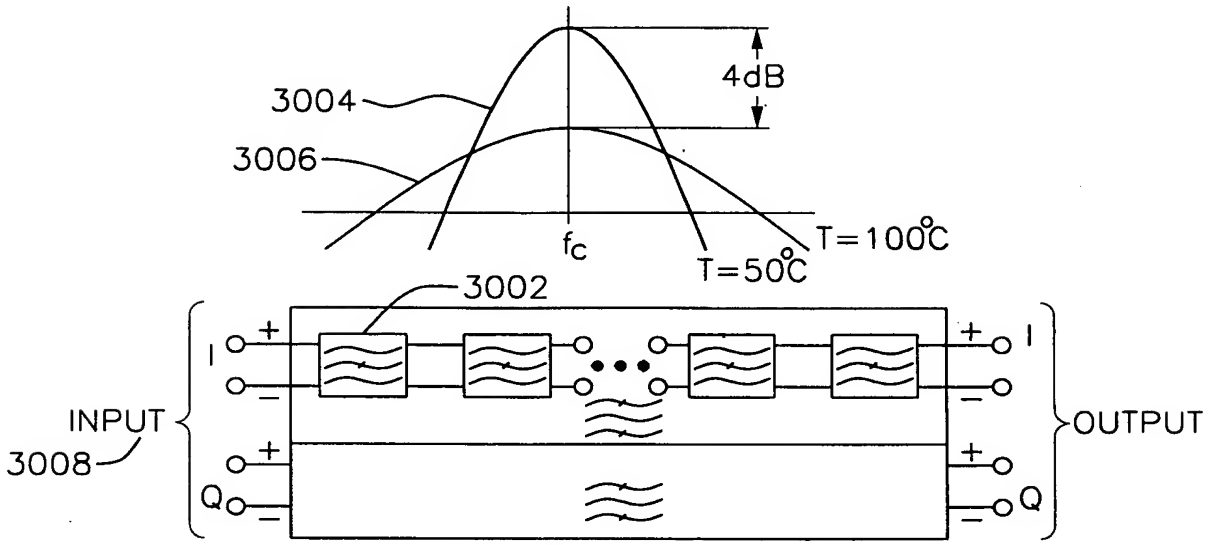

4dB
3004
3006
fc
T=100°C
T=50°C
3002
INPUT
3008
I
Q
OUTPUT

FIG.31

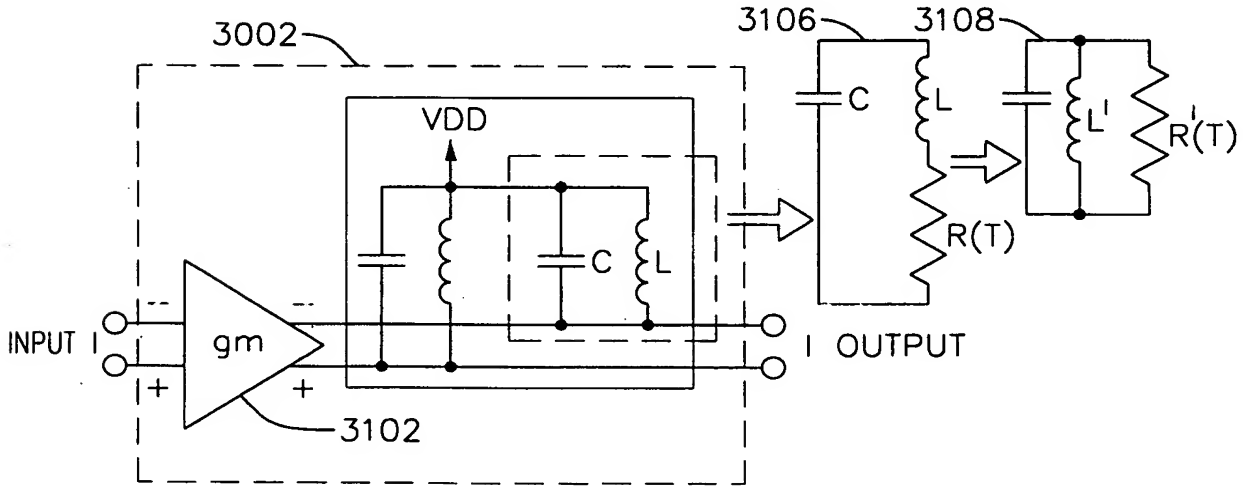
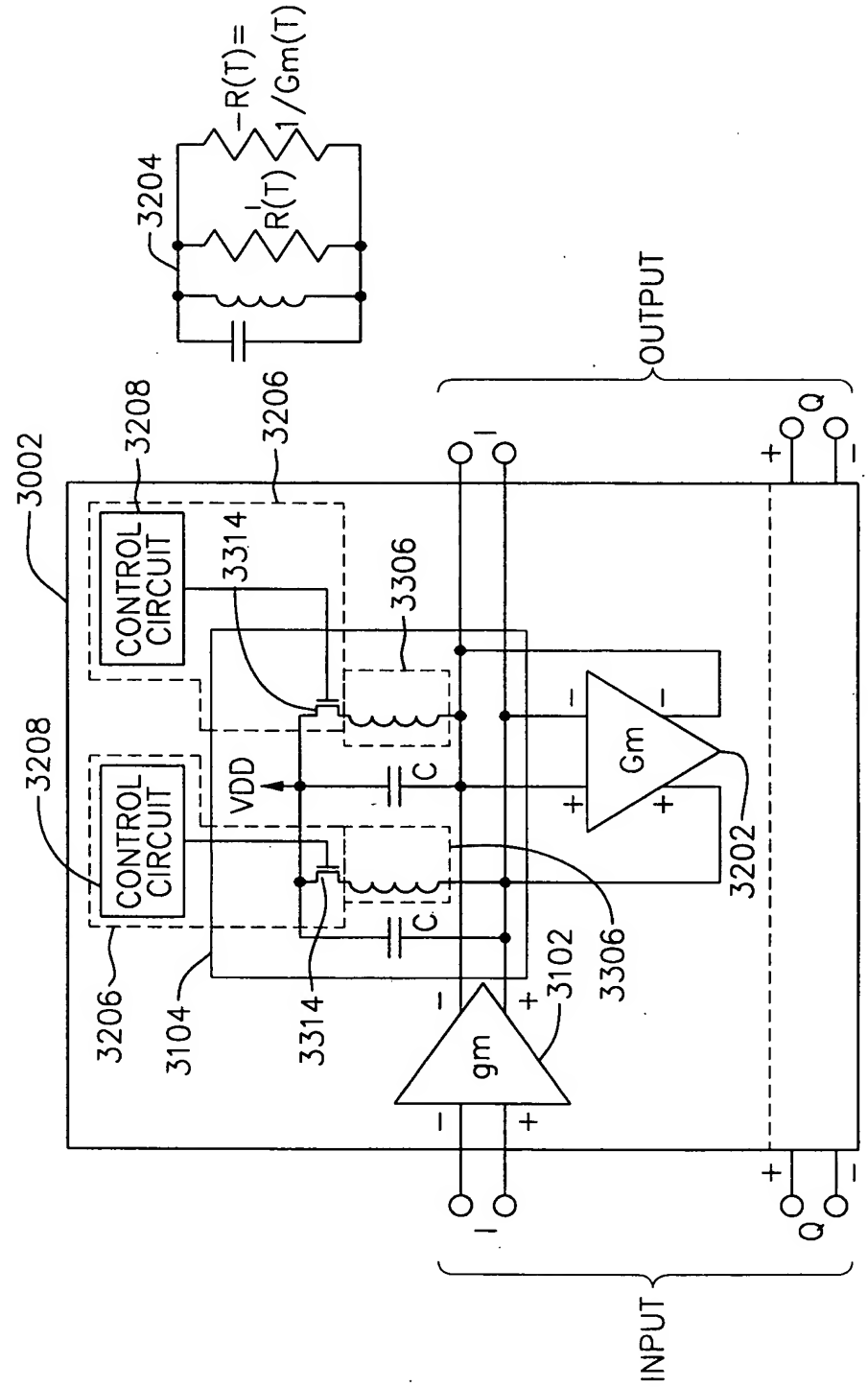

3002
3106
3108
VDD
C
L
R(T)
INPUT I
gm
3102
I OUTPUT

FIG.32


R(T)=
1/Gm(T)
3204
R(T)
OUTPUT
3002
3208
3206
CONTROL CIRCUIT
3314
3306
VDD
C
Gm
3202
3208
CONTROL CIRCUIT
3206
3104
3314
3102
3306
gm
Q
INPUT

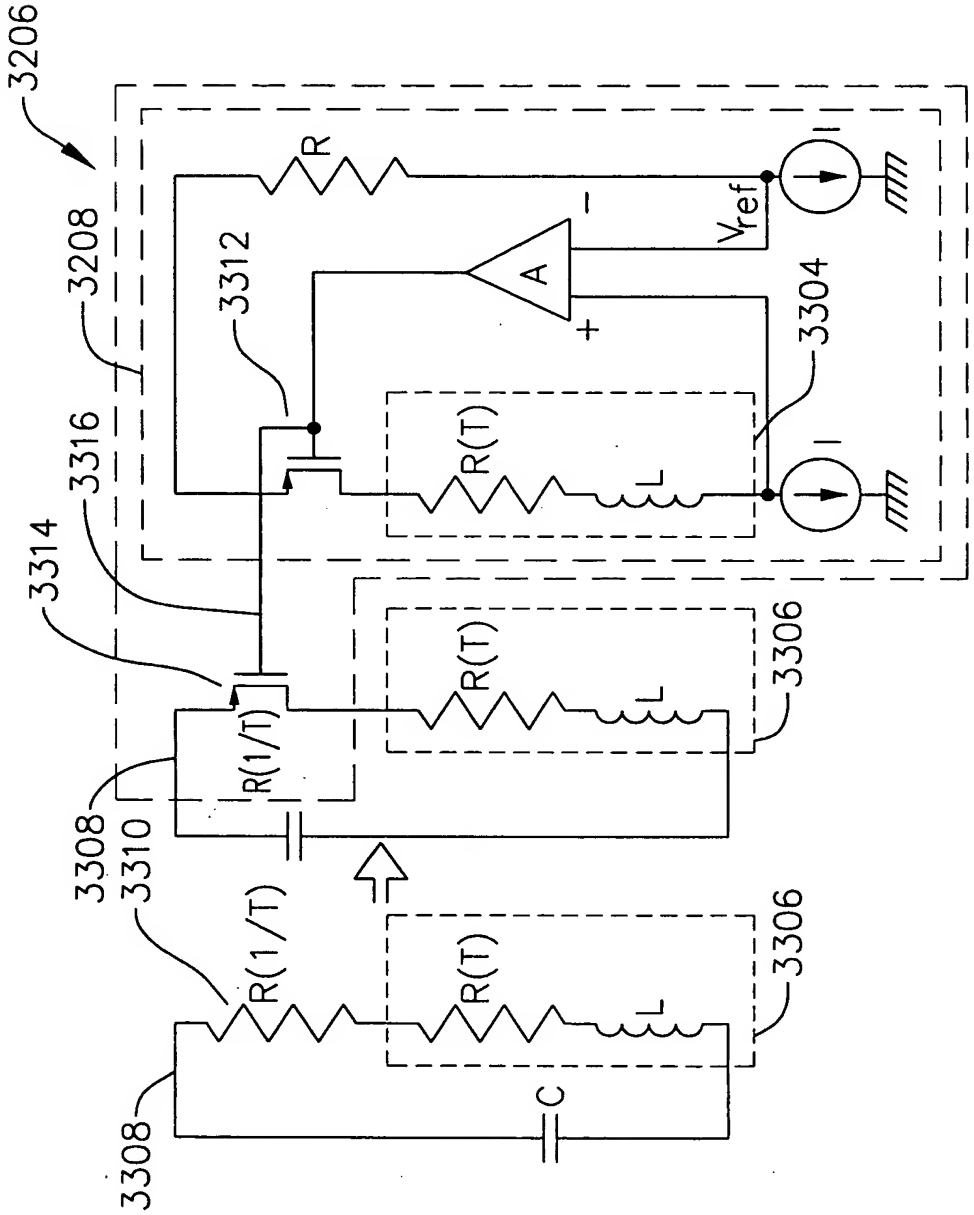

3206
3208
R
3312
A
Vref
I
3304
3316
R(T)
L
3314
3306
R(T)
L
R(1/T)
3308
3310
R(1/T)
3306
R(T)
L
C
3308

FIG.33

FIG.34

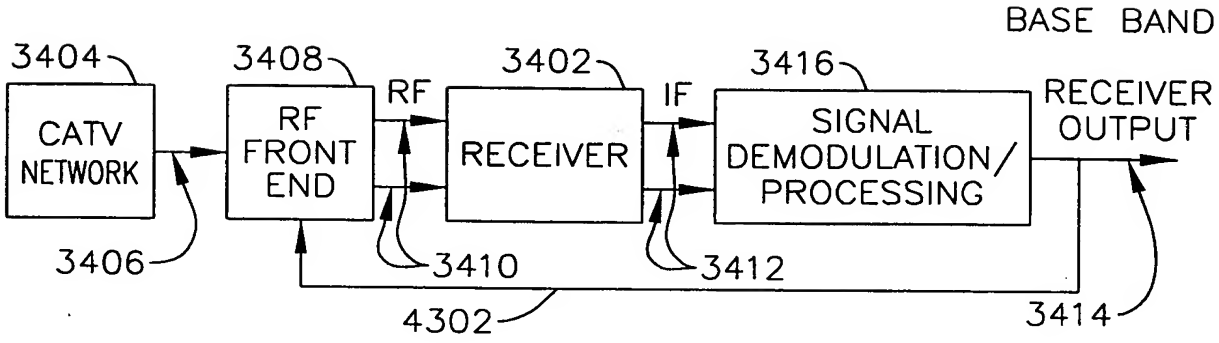

BASE BAND
3404
3408
3402
3416
CATV NETWORK
RF FRONT END
RF
RECEIVER
IF
SIGNAL DEMODULATION/ PROCESSING
RECEIVER OUTPUT
3406
3410
3412
4302
3414

FIG.35

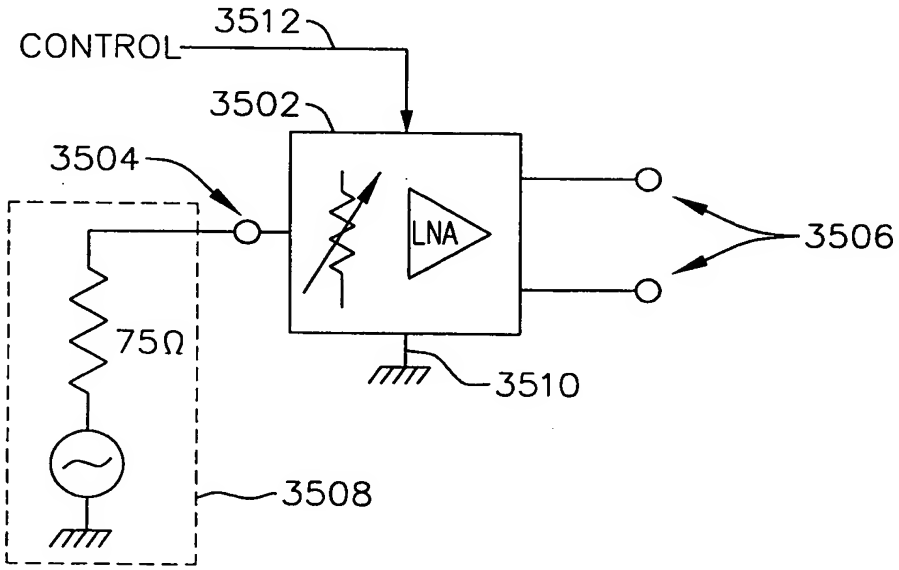

CONTROL
3512
3502
3504
LNA
3506
75Ω
3510
3508

FIG. 36

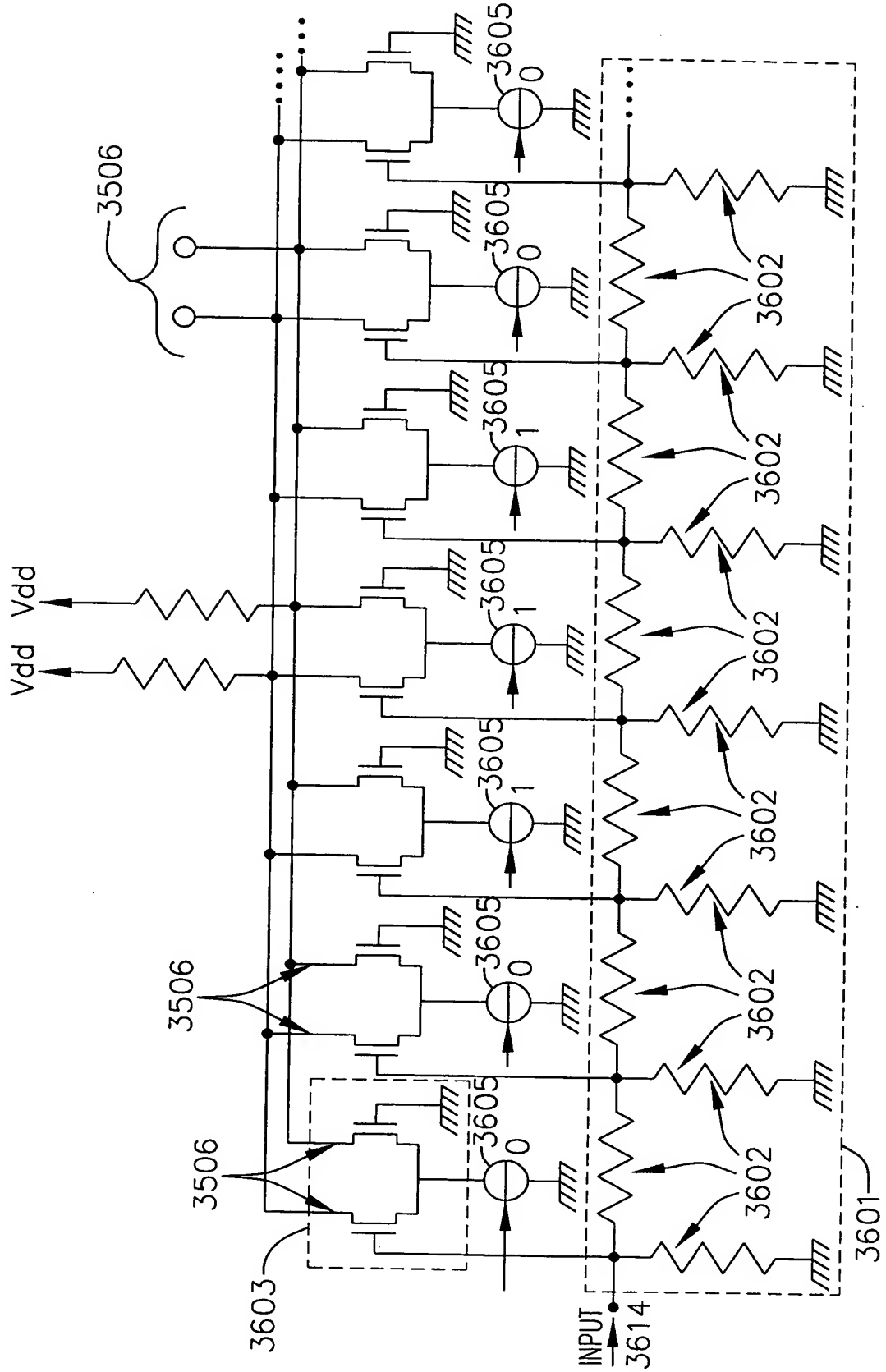


FIG.37

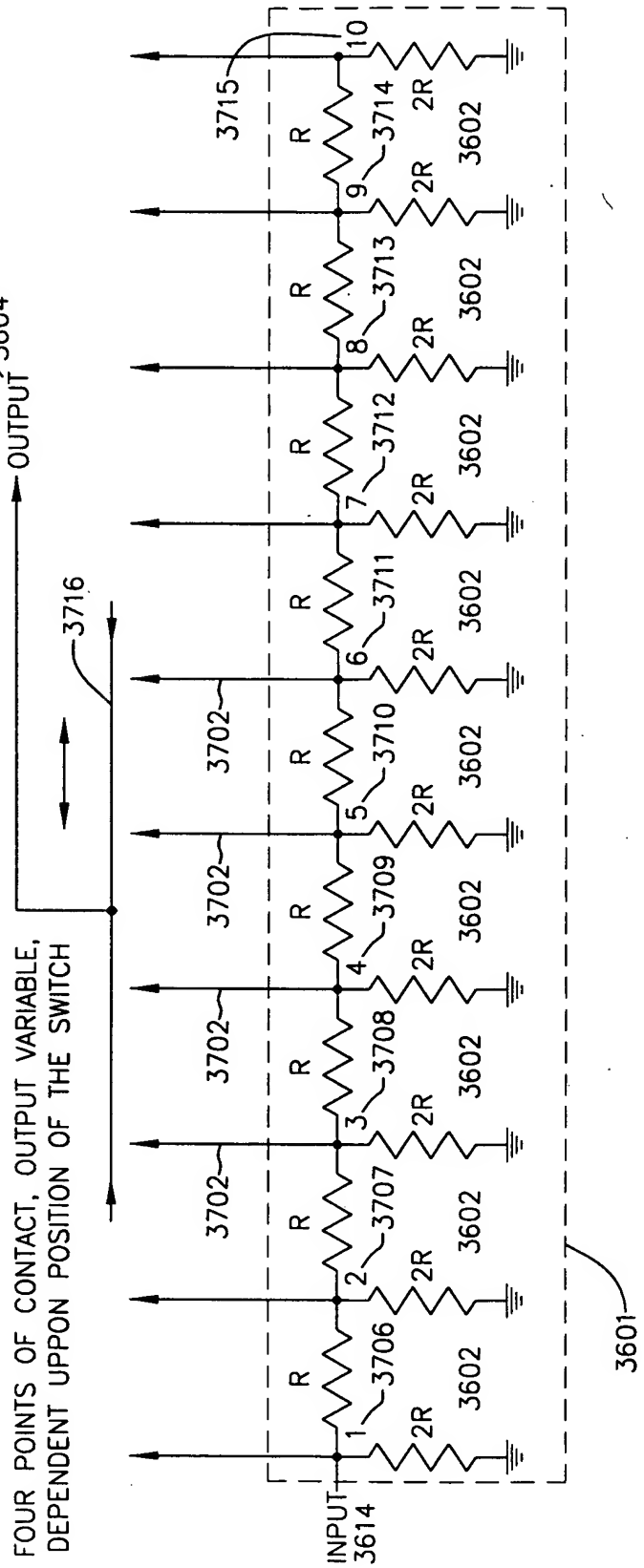
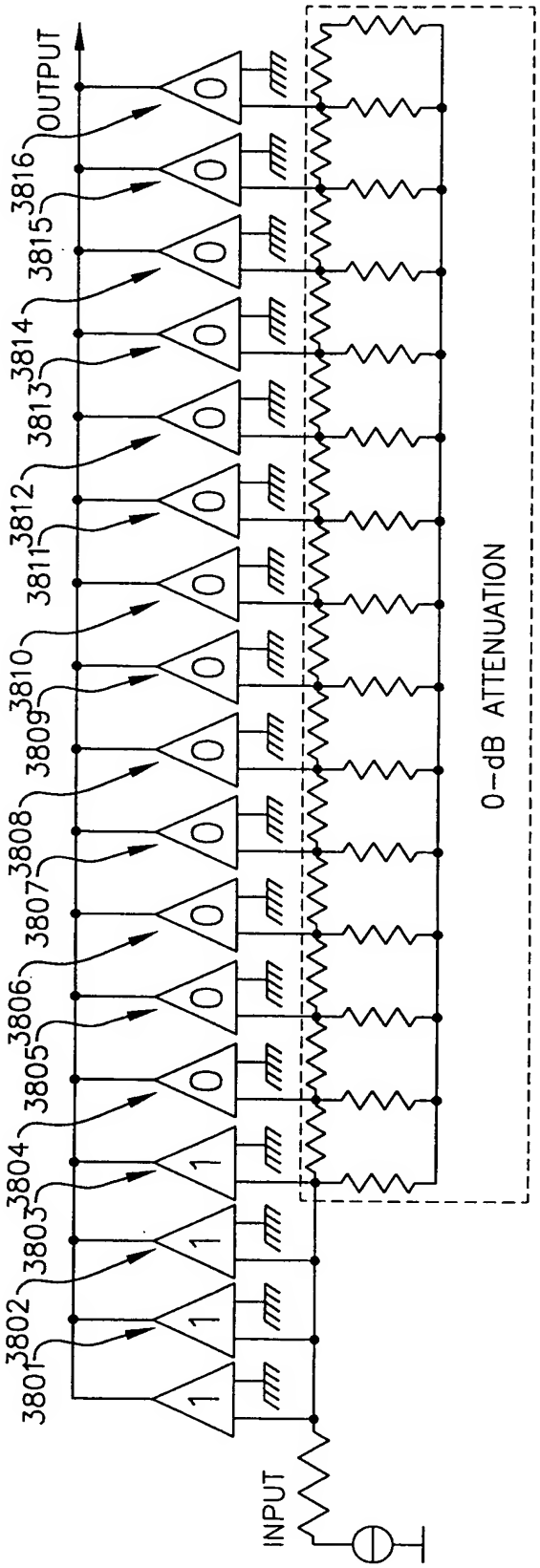

OUTPUT
3604
3716
FOUR POINTS OF CONTACT, OUTPUT VARIABLE, DEPENDENT UPPON POSITION OF THE SWITCH
INPUT
3614
3601
3715
R
2R
3602
3702
3706
3707
3708
3709
3710
3711
3712
3713
3714
1
2
3
4
5
6
7
8
9
10

FIG. 38


PGA SETTINGS
OUTPUT
INPUT
0-dB ATTENUATION
3801
3802
3803
3804
3805
3806
3807
3808
3809
3810
3811
3812
3813
3814
3815
3816
1
0

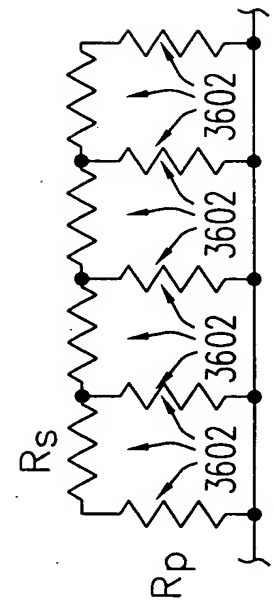

Rs
Rp
3602
3602
3602
3602
3602

FIG.39

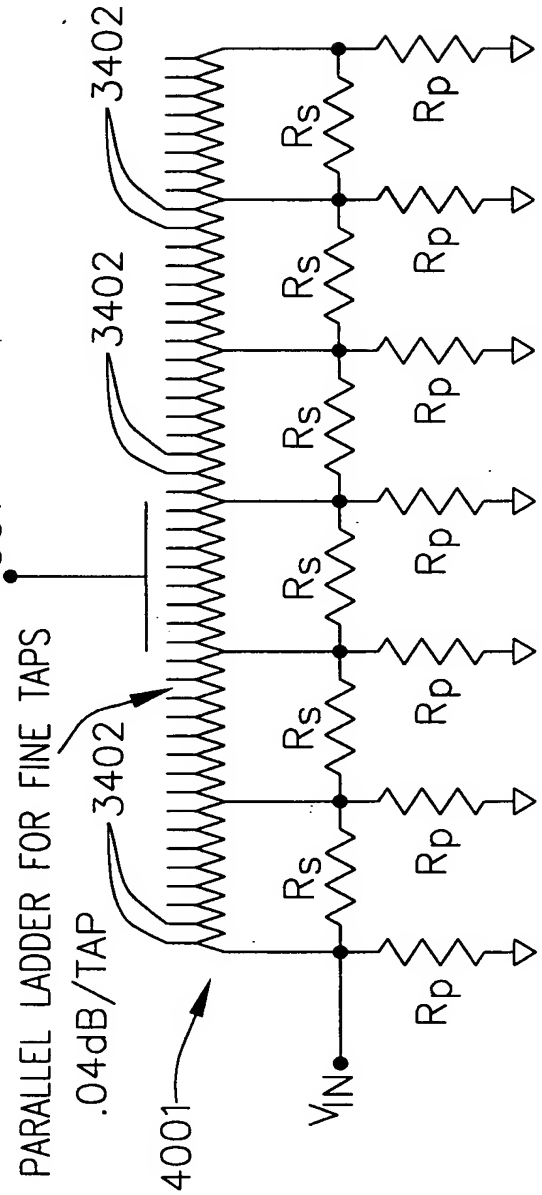

PGA ARCHITECTURE
VOUT
PARALLEL LADDER FOR FINE TAPS
.04dB/TAP
3402
3402
3402
4001
VIN
Rs
Rp

FIG.40

FIG. 41

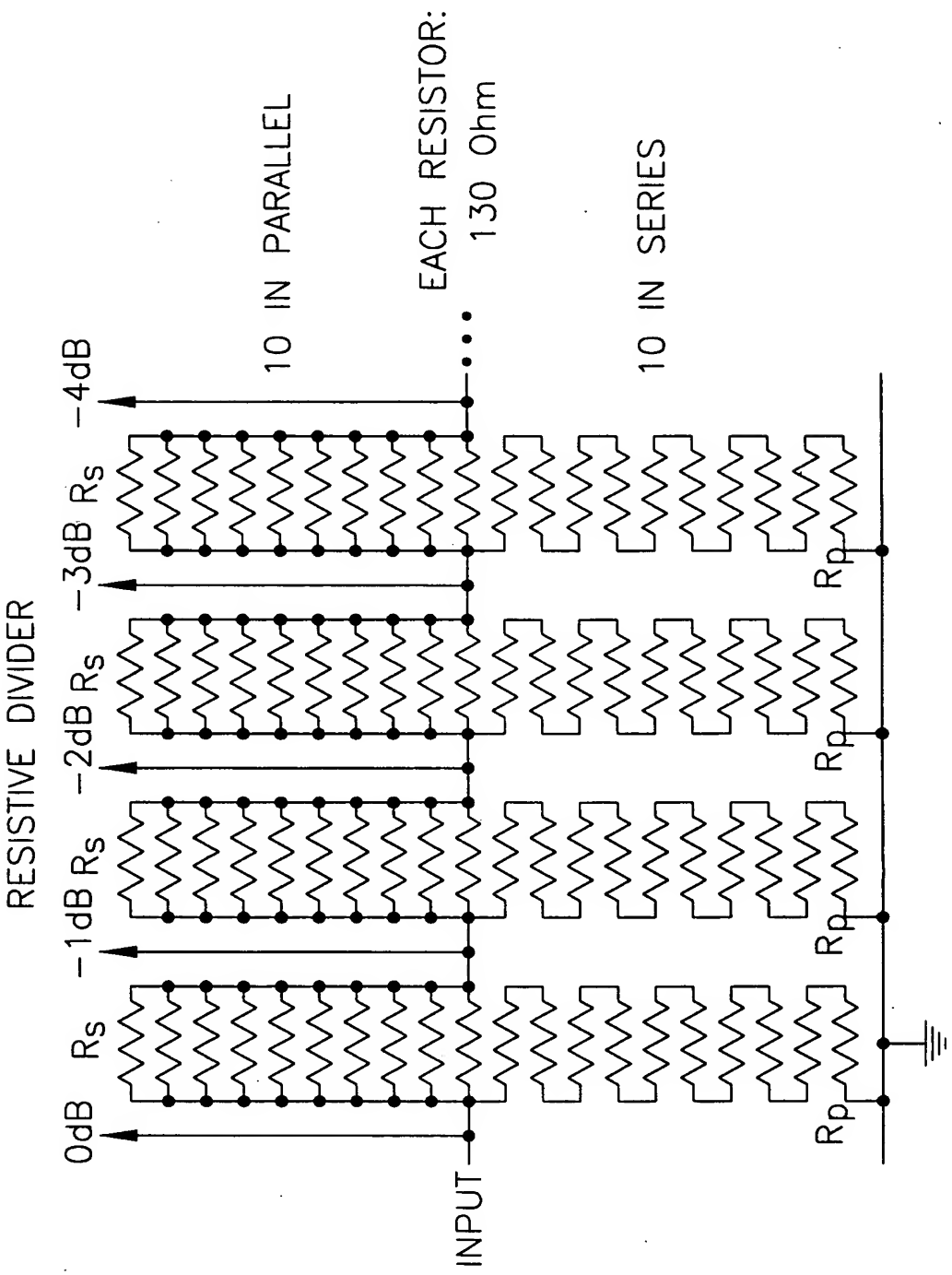

RESISTIVE DIVIDER
0dB Rs
-1dB Rs
-2dB Rs
-3dB Rs
-4dB
INPUT
10 IN PARALLEL
EACH RESISTOR:
130 Ohm
10 IN SERIES
Rp
Rp
Rp
Rp

FIG. 42

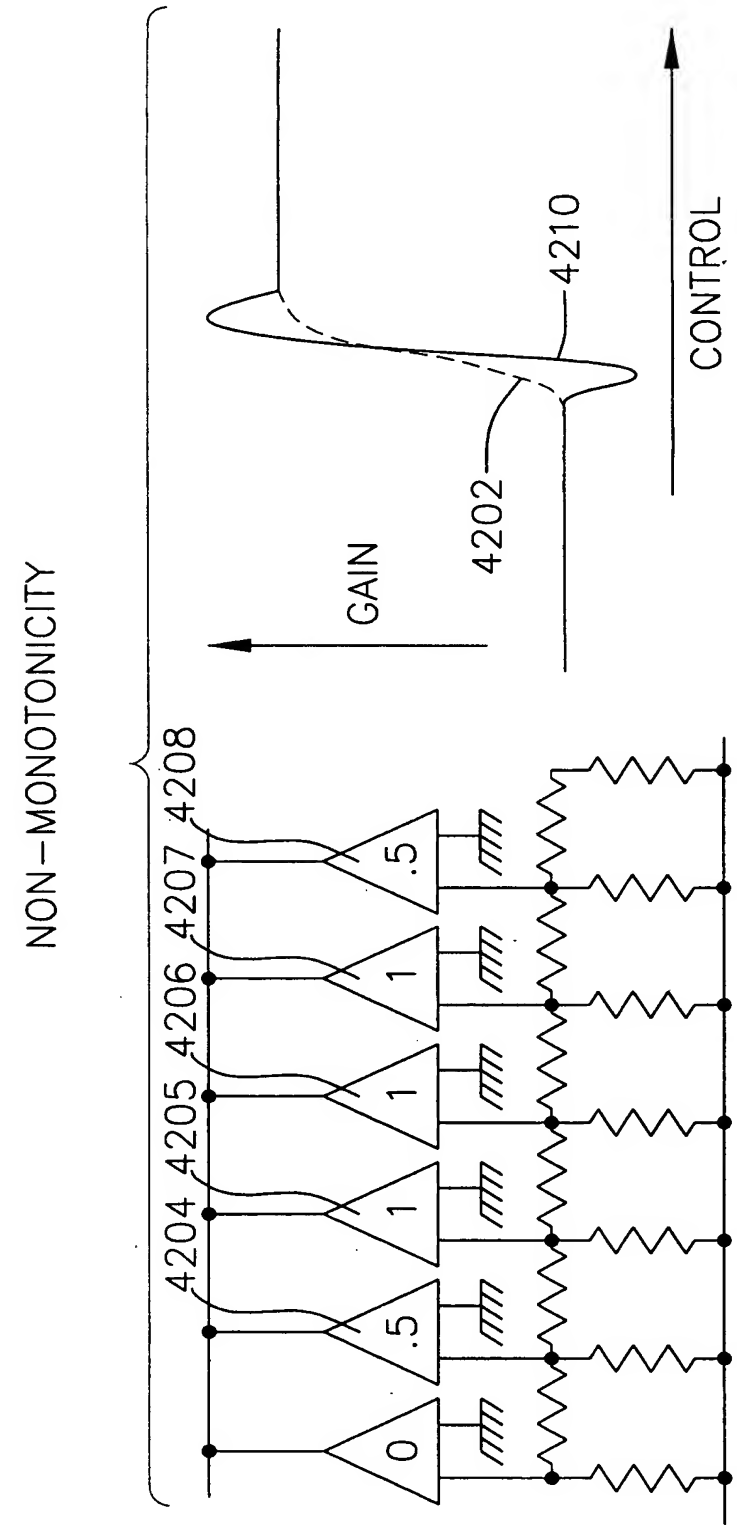

NON-MONOTONICITY
GAIN
CONTROL
4202
4210
4204
4205
4206
4207
4208
0
.5
1
1
1
.5

FIG. 43

CLAMPING CONTROL RANGE

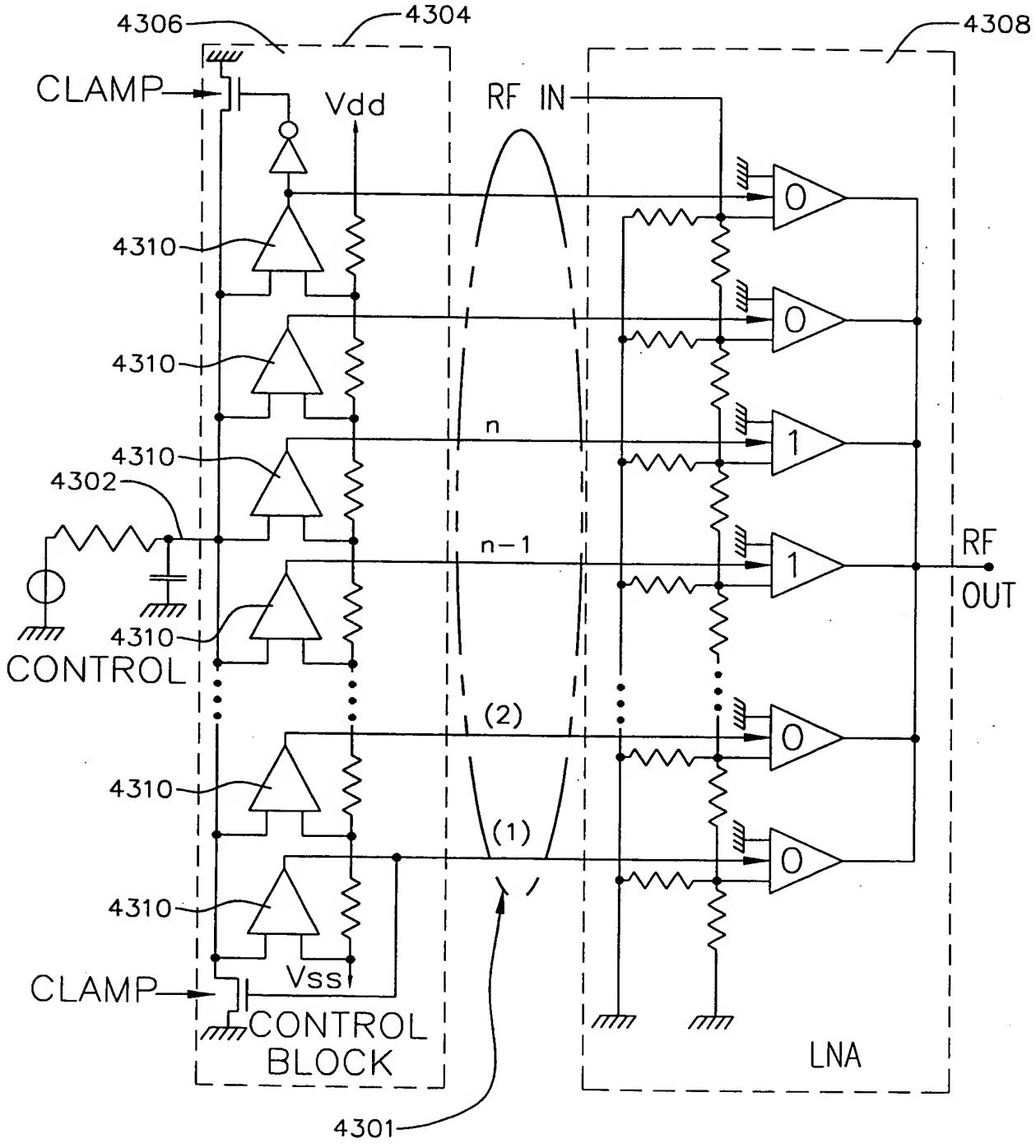
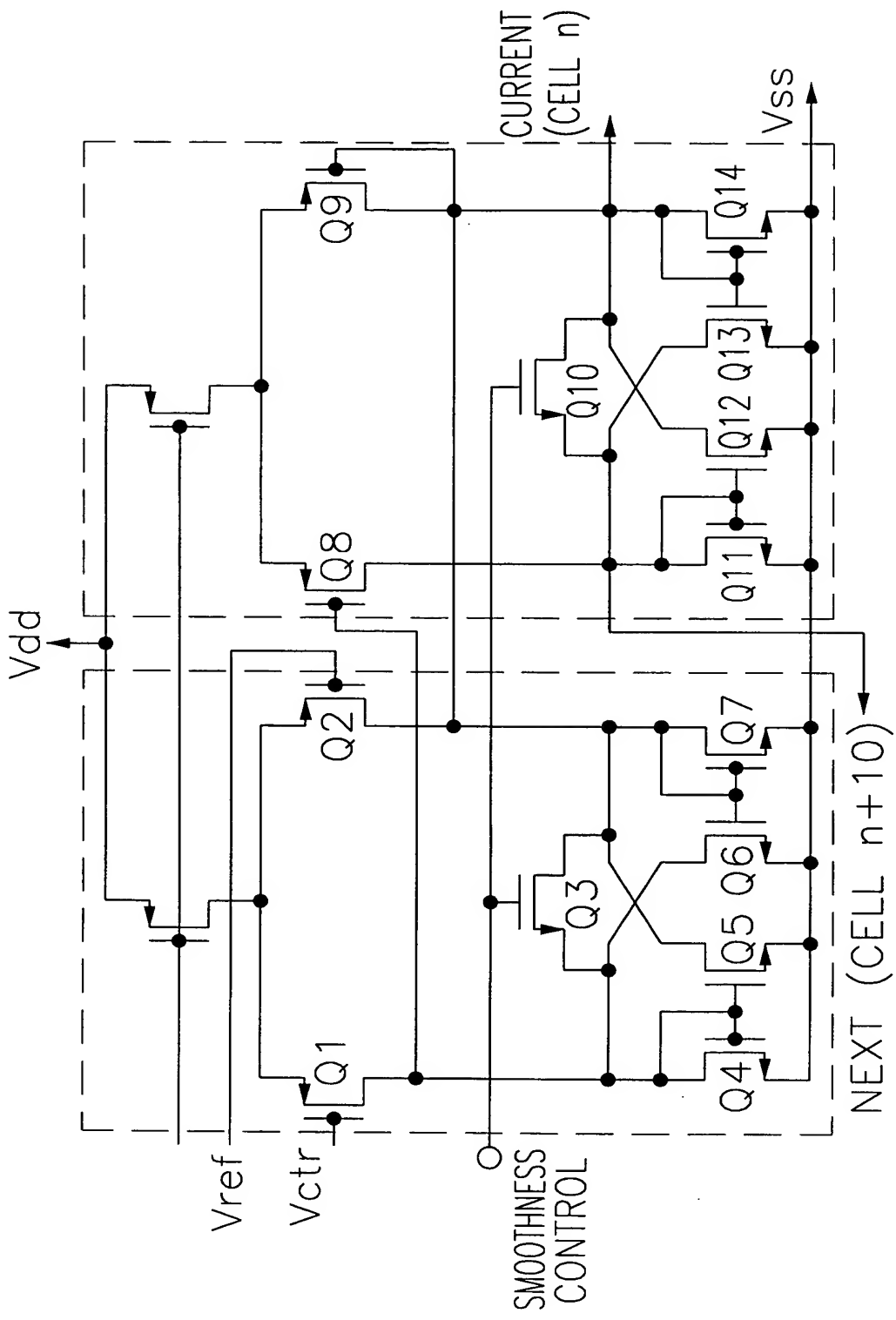


FIG. 44a

CONTROLLED GAIN COMPARATOR



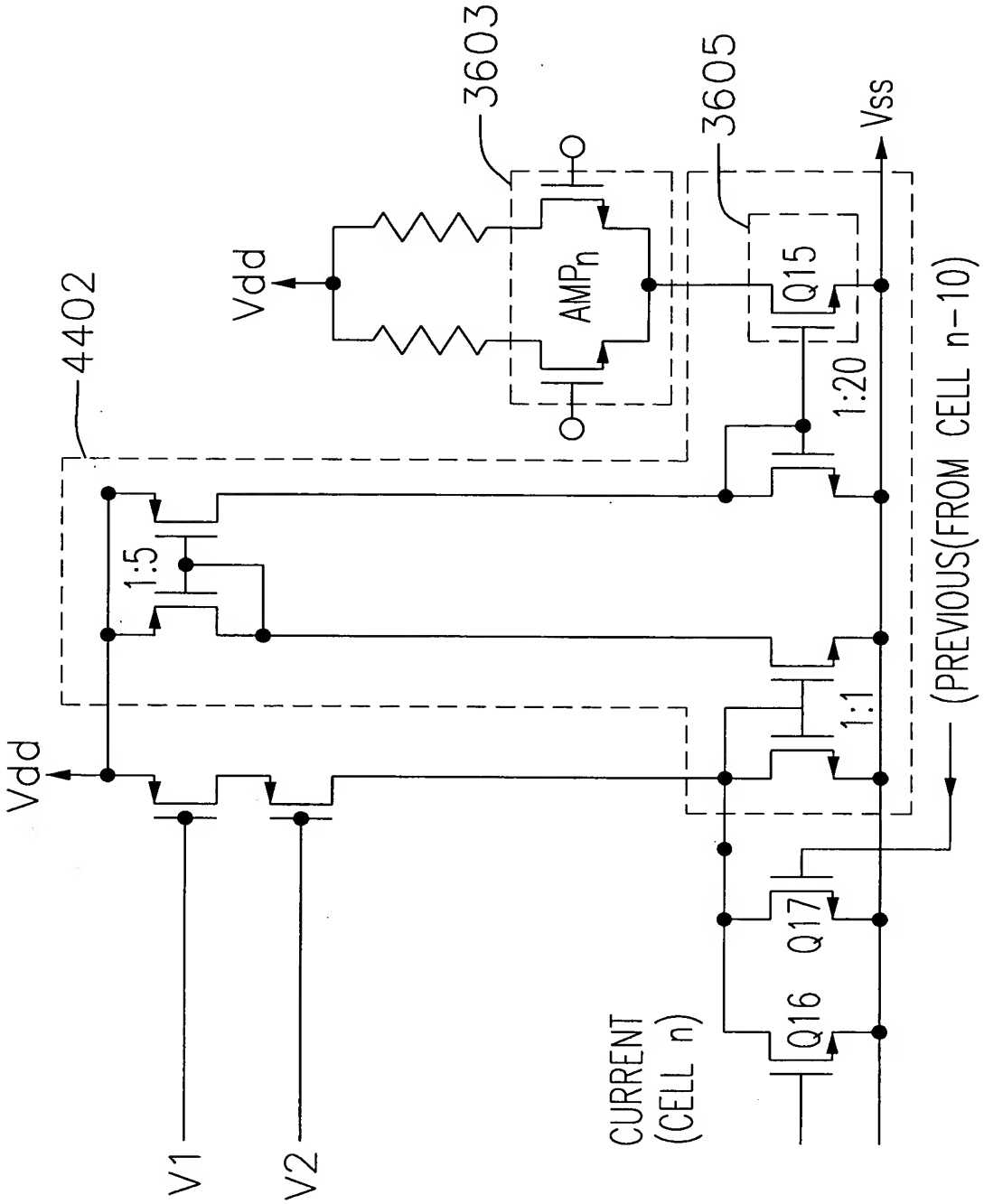
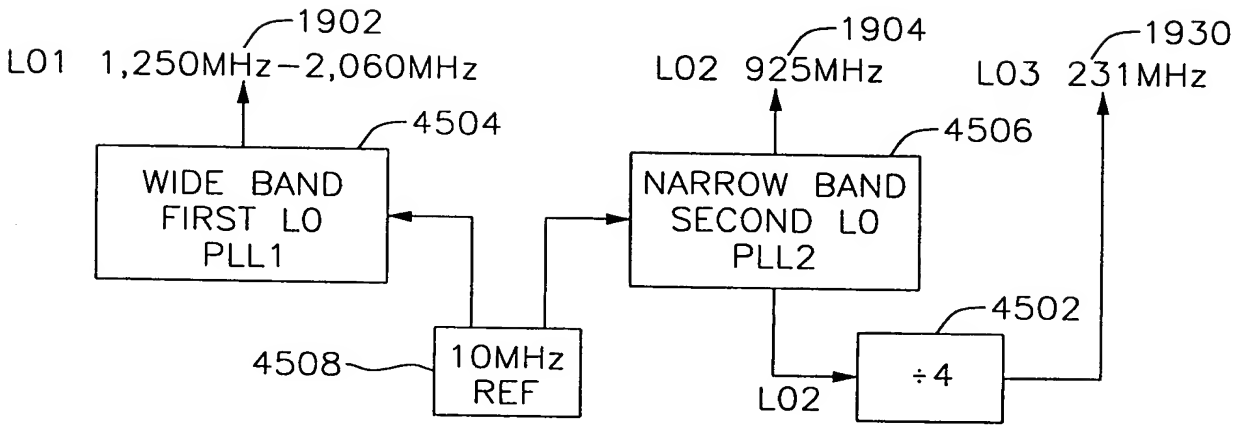

3603
3605
Vss
Vdd
AMPn
Q15
1:20
4402
1:5
1:1
(PREVIOUS(FROM CELL n-10)
Vdd
Q17
Q16
CURRENT
(CELL n)
V1
V2

FIG. 44b

FIG. 45


1902
L01 1,250MHz–2,060MHz
1904
L02 925MHz
1930
L03 231MHz
4504
WIDE BAND FIRST LO PLL1
4506
NARROW BAND SECOND LO PLL2
4502
÷4
L02
4508
10MHz REF

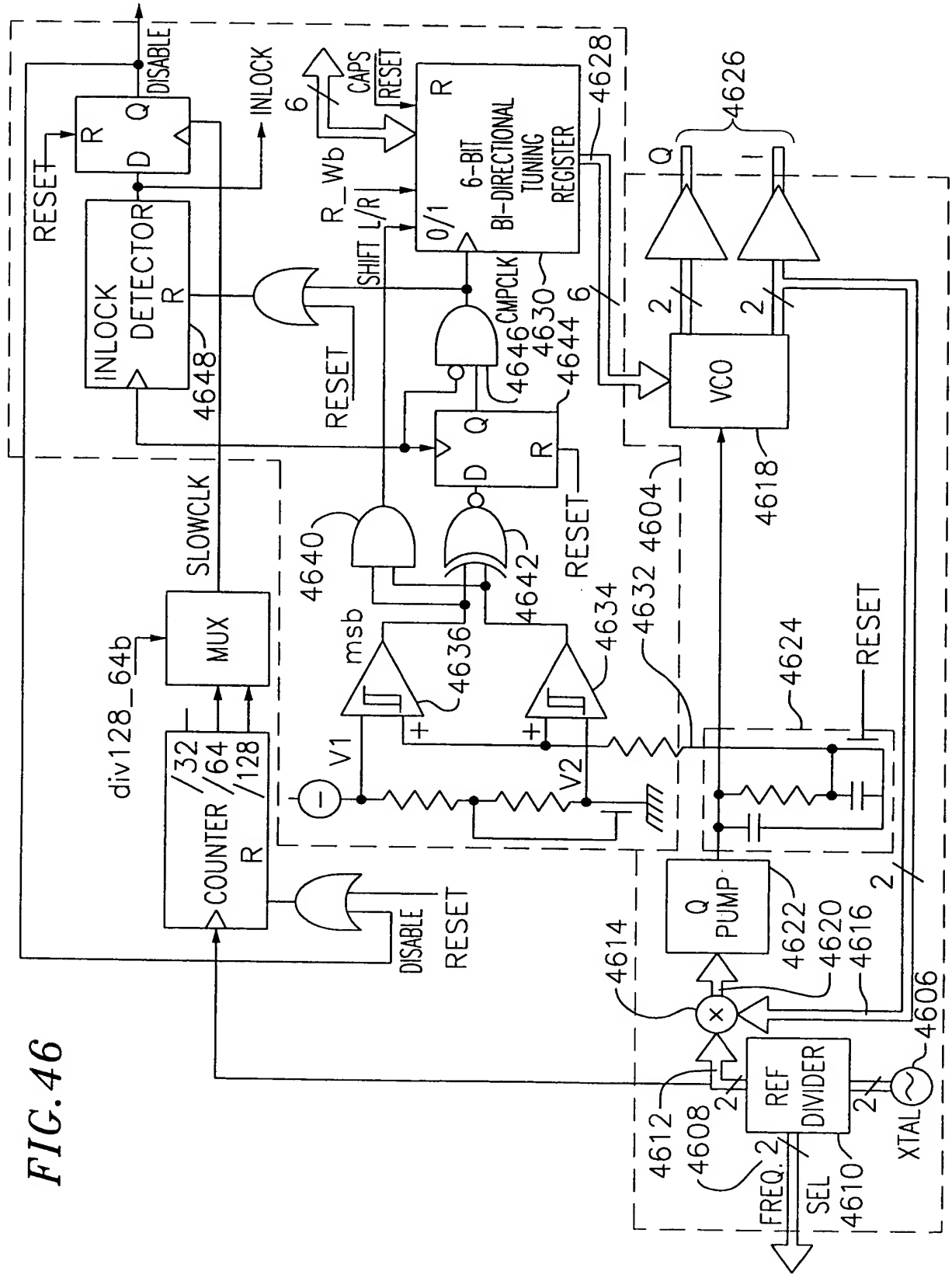
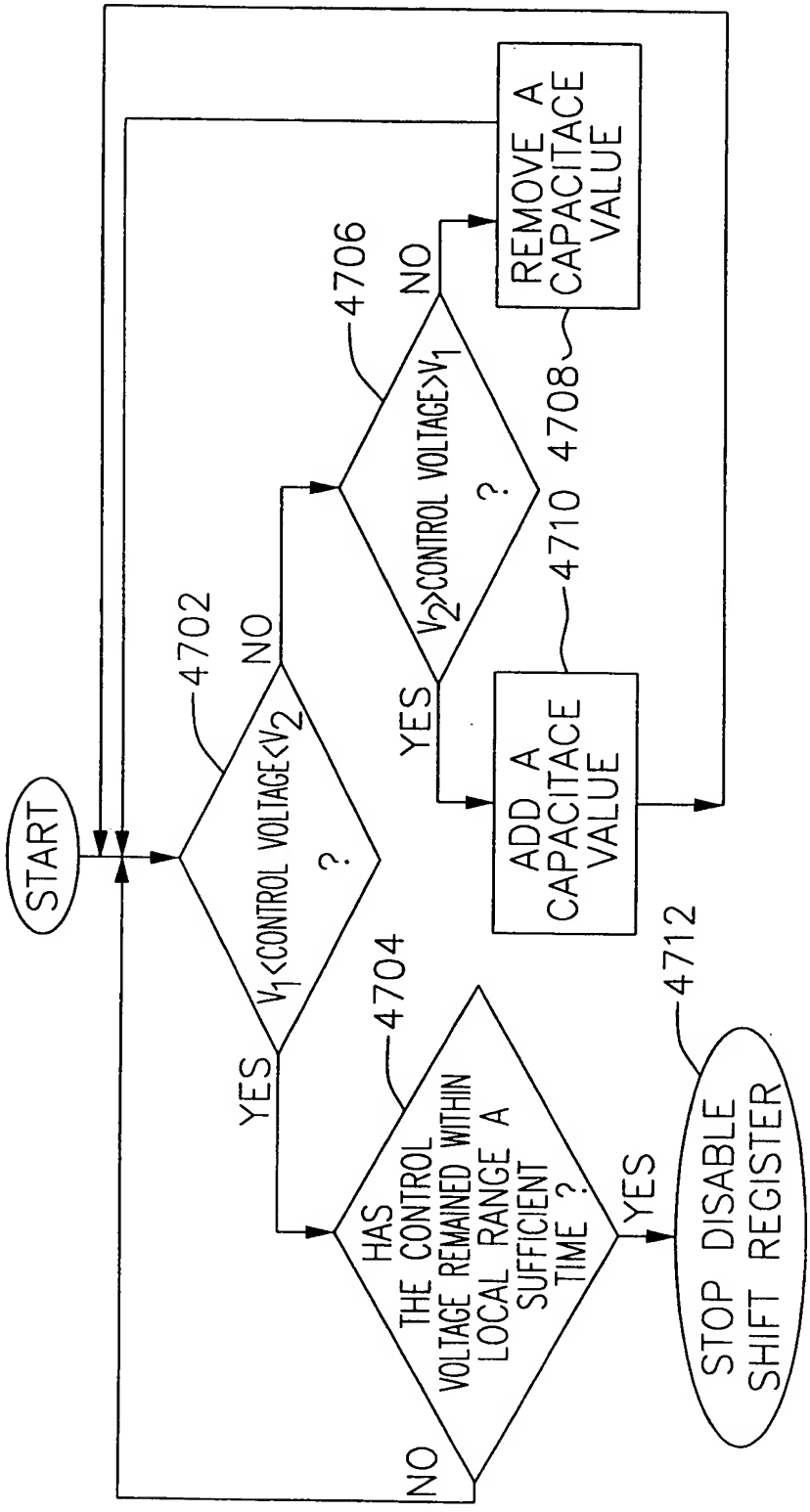

DISABLE
INLOCK
RESET
CAPS
RESET
6
R
Q
D
6-BIT
BI-DIRECTIONAL
TUNING
REGISTER
4628
4626
R_Wb
0/1
SHIFT L/R
INLOCK
DETECTOR
R
4648
RESET
CMPCLK
4630
6
4646
4644
VCO
2
2
SLOWCLK
4640
4642
RESET
4632
4604
4618
MUX
msb
4636
4634
4624
RESET
div128_64b
/32
/64
/128
V1
V2
COUNTER
R
DISABLE
RESET
Q
PUMP
4614
4622
4620
4616
2
4606
REF
DIVIDER
2
2
4612
4608
FREQ. 2
SEL
4610
XTAL

FIG. 46

FIG. 47


START
4702
V_1<CONTROL VOLTAGE<V_2 ?
NO
YES
4704
HAS THE CONTROL VOLTAGE REMAINED WITHIN LOCAL RANGE A SUFFICIENT TIME ?
NO
YES
4706
V_2>CONTROL VOLTAGE>V_1 ?
NO
YES
4708
REMOVE A CAPACITACE VALUE
4710
ADD A CAPACITACE VALUE
4712
STOP DISABLE SHIFT REGISTER

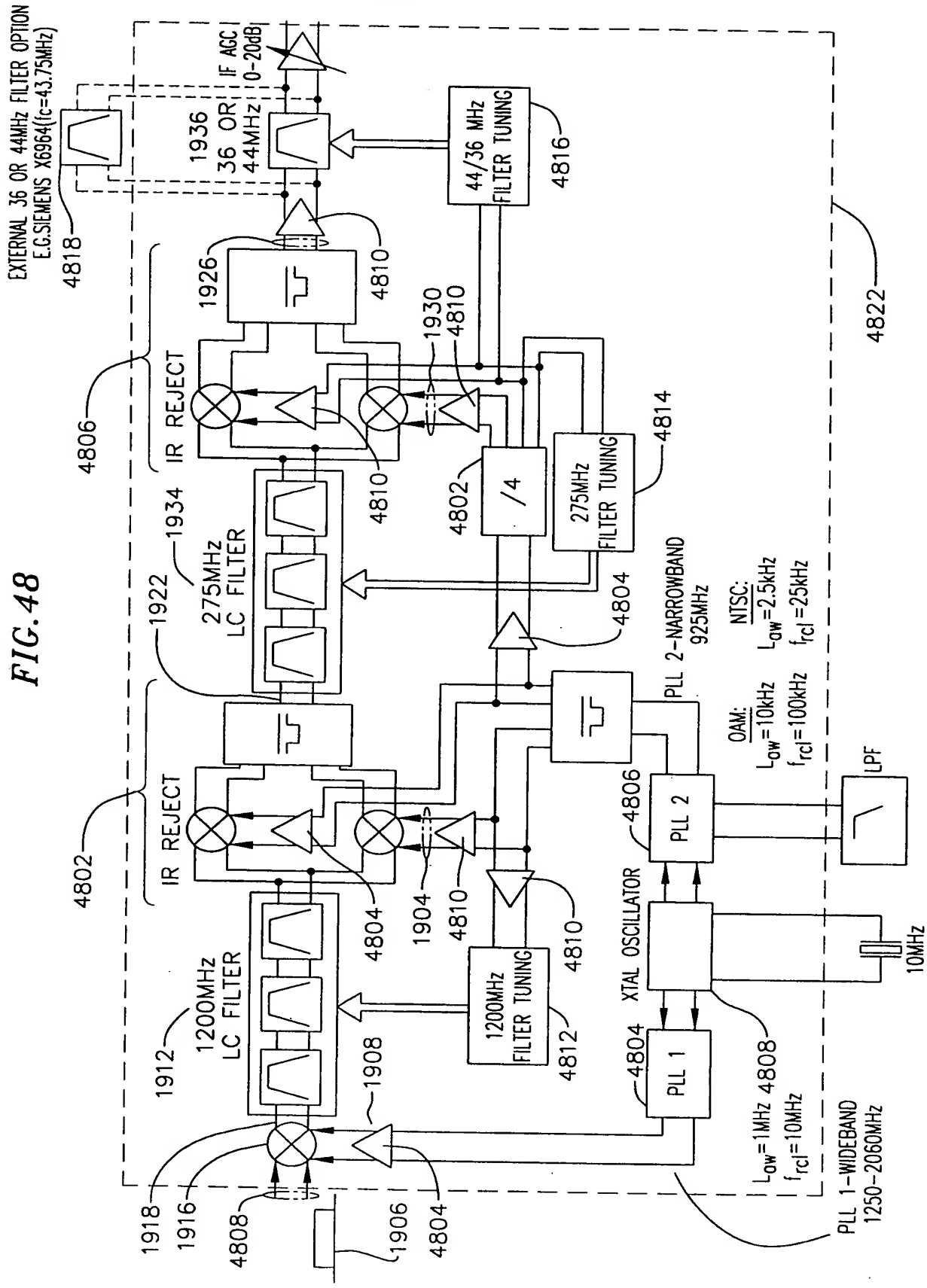

EXTERNAL 36 OR 44MHz FILTER OPTION
E.G.SIEMENS X6964(fc=43.75MHz)
4818
1936
36 OR 44MHz
IF AGC 0-20dB
44/36 MHz FILTER TUNING
4816
4810
1926
1930
4810
4822
4806
IR REJECT
4814
275MHz FILTER TUNING
4802
/4
1934
275MHz LC FILTER
4804
1922
PLL 2-NARROWBAND 925MHz
NTSC: Low=2.5kHz frcl=25kHz
OAM: Low=10kHz frcl=100kHz
LPF
4806
PLL 2
4802
IR REJECT
4804
1904
4810
4810
XTAL OSCILLATOR
10MHz
1200MHz LC FILTER
1912
1908
1200MHz FILTER TUNING
4812
4804
PLL 1
4808
Low=1MHz 4808
frcl=10MHz
1918
1916
4808
1906
4804
PLL 1-WIDEBAND 1250-2060MHz

FIG. 48

FIG. 49

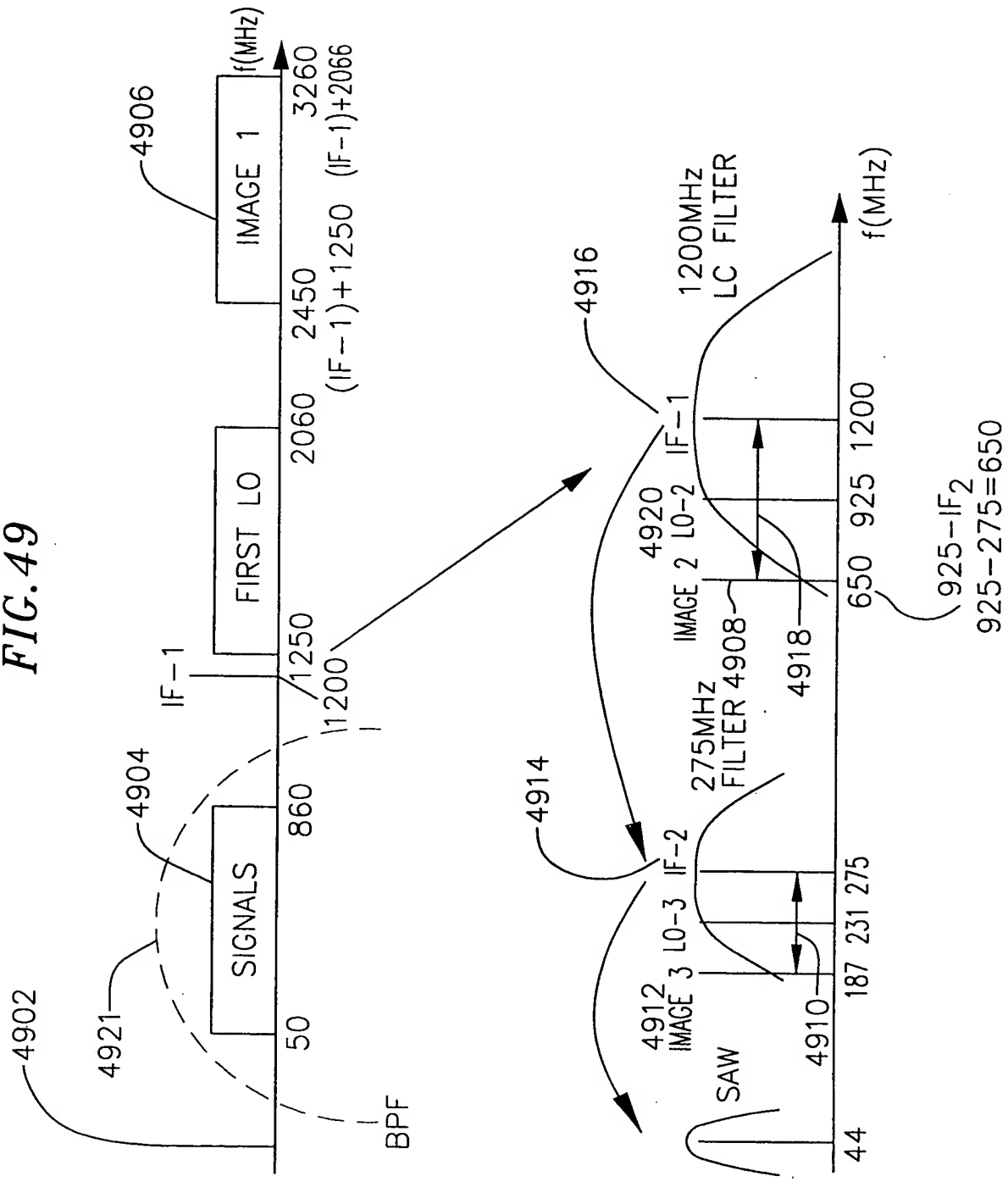

4902
4921
4904
4906
4914
4916
4910
4912
4918
4920
4908
SIGNALS
IMAGE 1
FIRST LO
IF-1
IF-2
LO-3
LO-2
IMAGE 3
IMAGE 2
SAW
BPF
275MHz FILTER
1200MHz LC FILTER
f(MHz)
50
860
1200
1250
2060
2450
3260
(IF-1)+1250
(IF-1)+2066
44
187
231
275
650
925
1200
925-IF2
925-275=650

FIG. 50

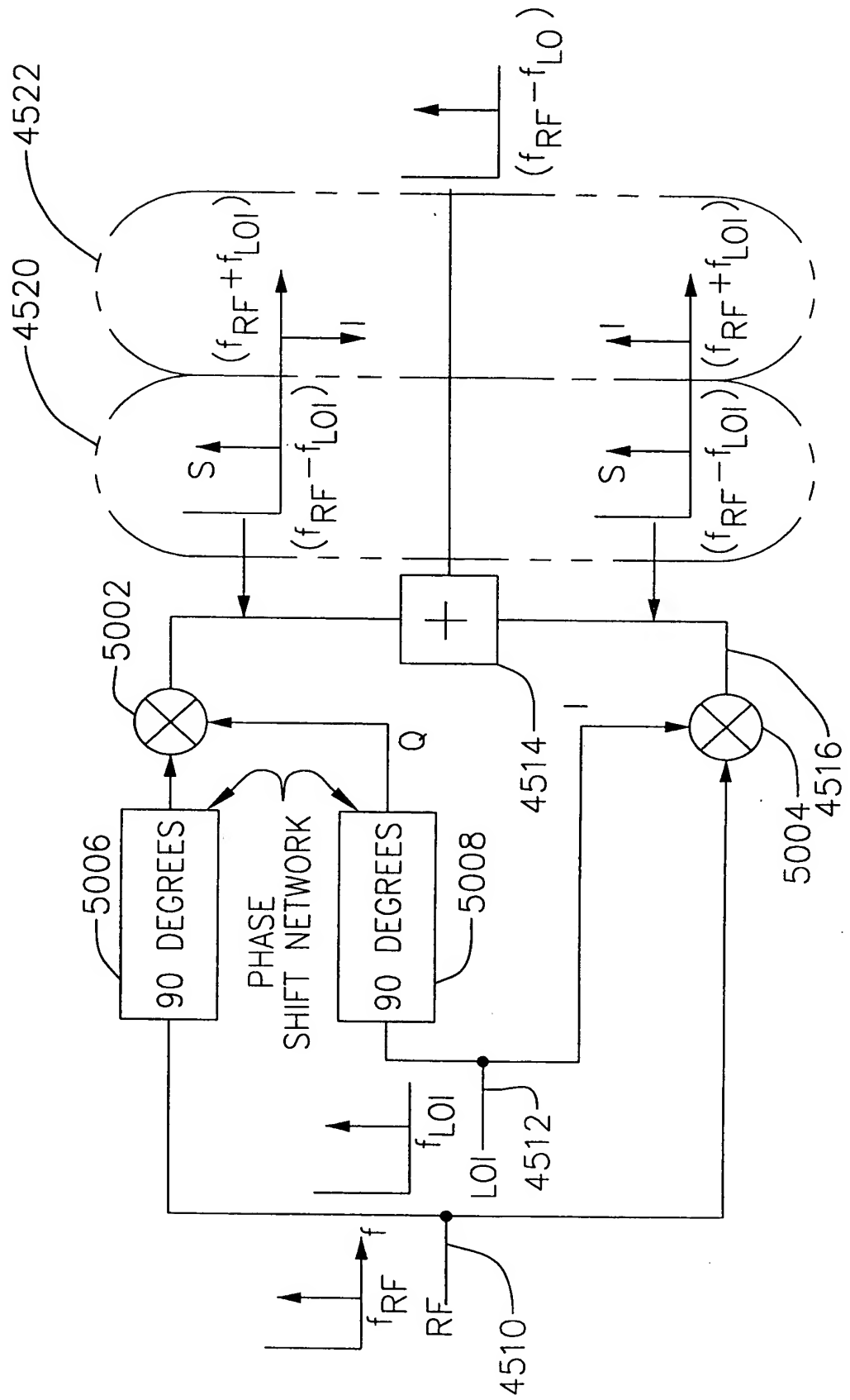

4522
4520
$(f_{RF}-f_{LO})$
$(f_{RF}+f_{LOI})$
I
S
$(f_{RF}-f_{LOI})$
5002
Q
4514
5004
4516
5006
90 DEGREES
PHASE SHIFT NETWORK
90 DEGREES
5008
f_{LOI}
LOI
4512
f_{RF}
RF
4510

FIG.51

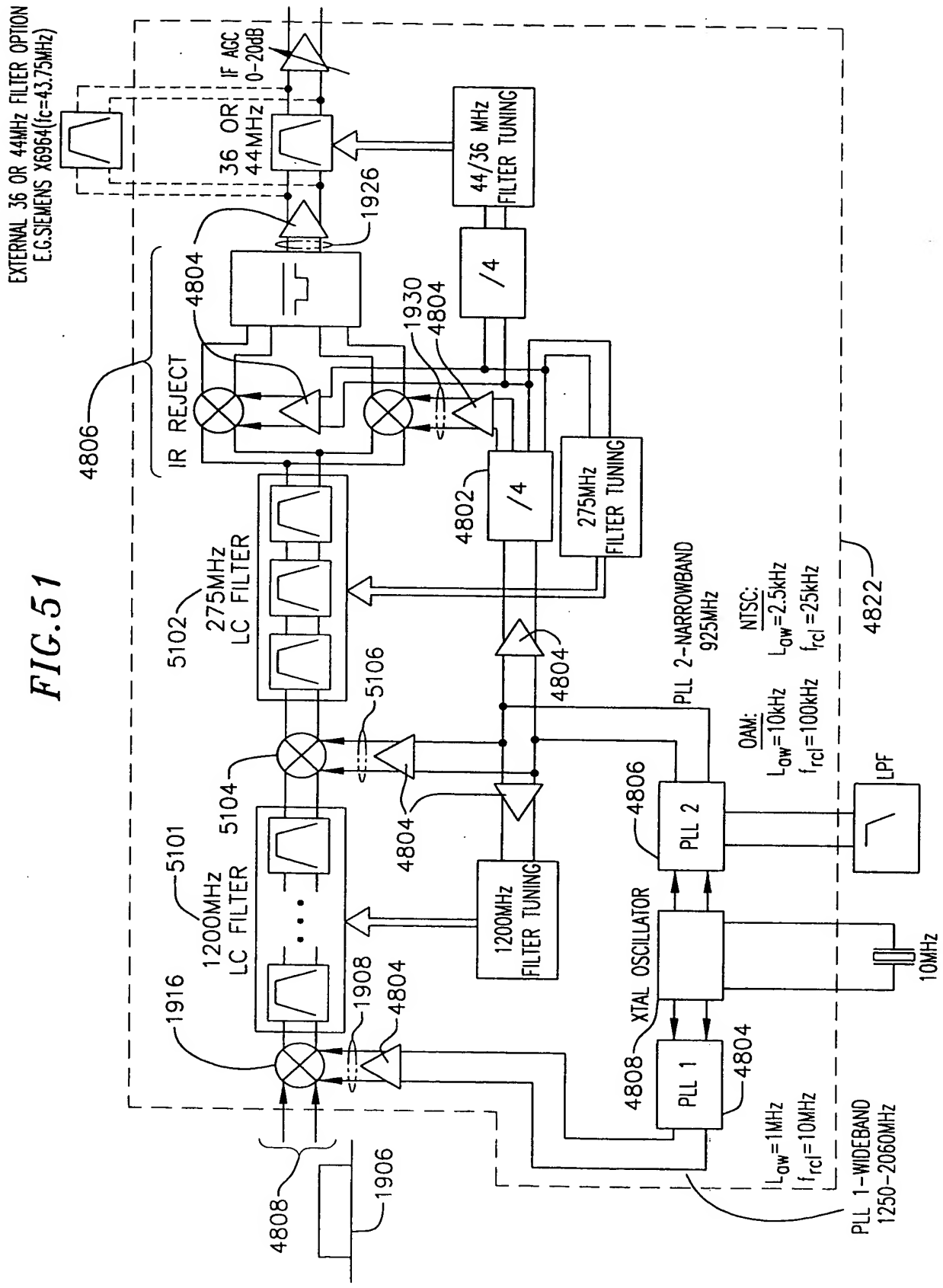
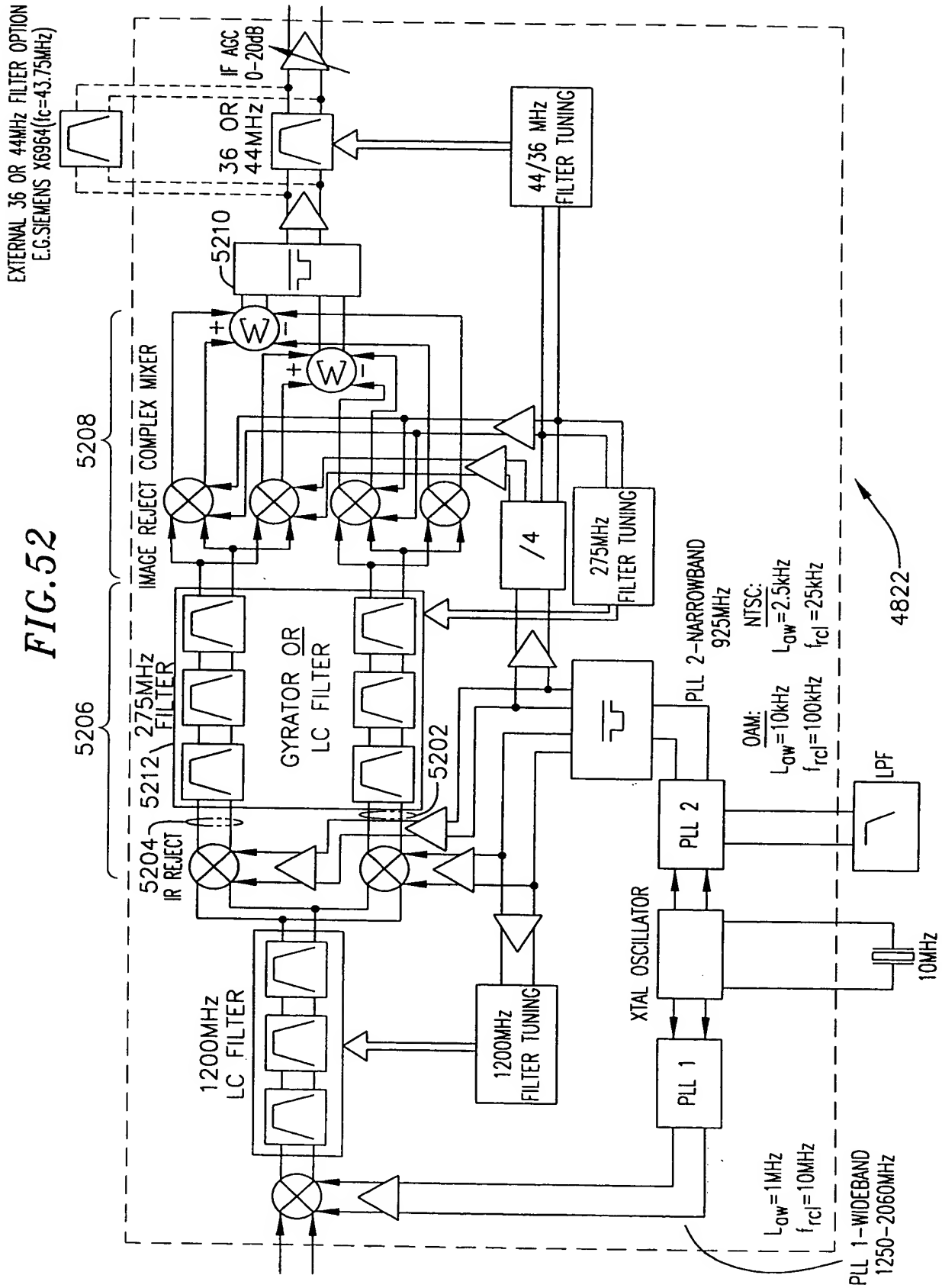

EXTERNAL 36 OR 44MHz FILTER OPTION
E.G.SIEMENS X6964(fc=43.75MHz)
IF AGC
0-20dB
36 OR
44MHz
1926
44/36 MHz
FILTER TUNING
/4
4804
1930
4804
IR REJECT
4806
4802
/4
275MHz
FILTER TUNING
5102
275MHz
LC FILTER
5106
4804
PLL 2-NARROWBAND
925MHz
NTSC:
Low=2.5kHz
frcl=25kHz
4822
OAM:
Low=10kHz
frcl=100kHz
5104
5101
1200MHz
LC FILTER
4804
4806
PLL 2
LPF
1916
1908
4804
1200MHz
FILTER TUNING
XTAL OSCILLATOR
10MHz
4808
PLL 1
4804
Low=1MHz
frcl=10MHz
4808
1906
PLL 1-WIDEBAND
1250-2060MHz

FIG. 52


EXTERNAL 36 OR 44MHz FILTER OPTION
E.G.SIEMENS X6964(fc=43.75MHz)
IF AGC 0-20dB
36 OR 44MHz
44/36 MHz FILTER TUNING
5210
5208
IMAGE REJECT COMPLEX MIXER
/4
275MHz FILTER TUNING
5206
5212
275MHz FILTER
GYRATOR OR LC FILTER
5202
PLL 2-NARROWBAND 925MHz
NTSC:
L_{ow}=2.5kHz
f_{rcl}=25kHz
OAM:
L_{ow}=10kHz
f_{rcl}=100kHz
4822
5204
IR REJECT
PLL 2
LPF
1200MHz LC FILTER
1200MHz FILTER TUNING
XTAL OSCILLATOR
10MHz
PLL 1
L_{ow}=1MHz
f_{rcl}=10MHz
PLL 1-WIDEBAND 1250-2060MHz

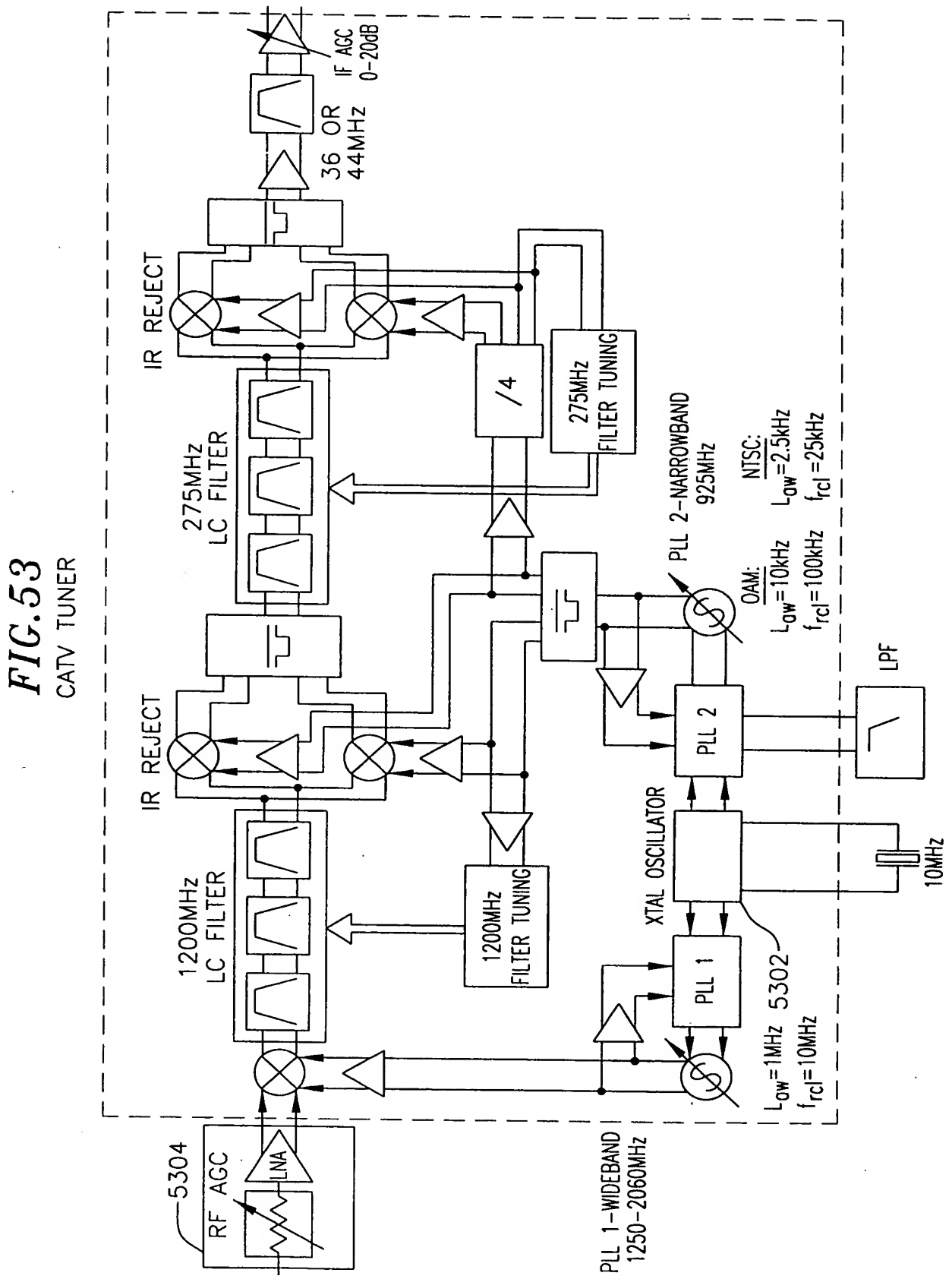
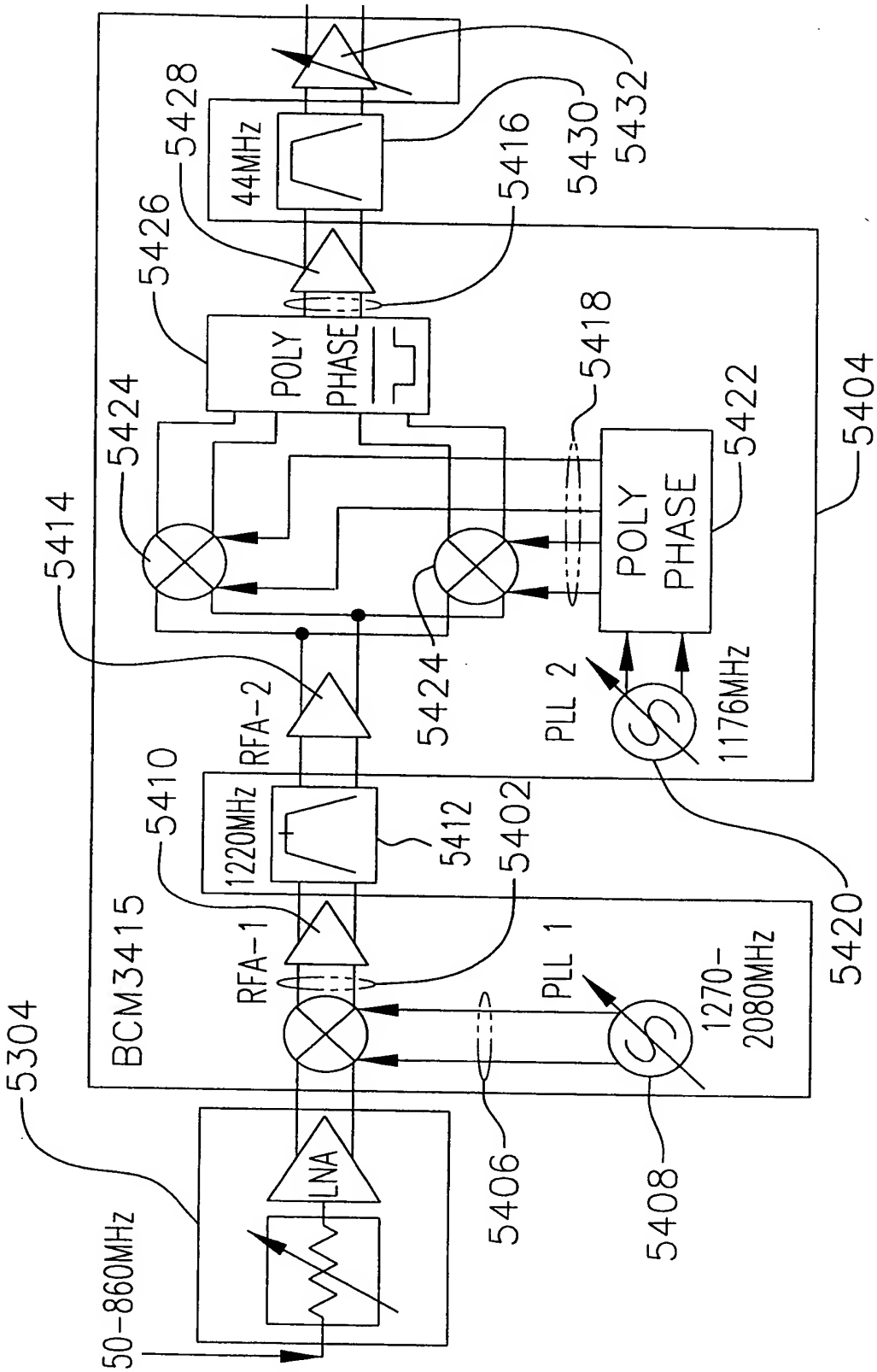


FIG.53
CATV TUNER

FIG.54


5304
BCM3415
5414
5424
5410
5412
5402
5404
5422
5418
5426
5428
5416
5430
5432
5420
5406
5408
50-860MHz
LNA
RFA-1
RFA-2
1220MHz
44MHz
POLY PHASE
PLL 1
PLL 2
1270-2080MHz
1176MHz

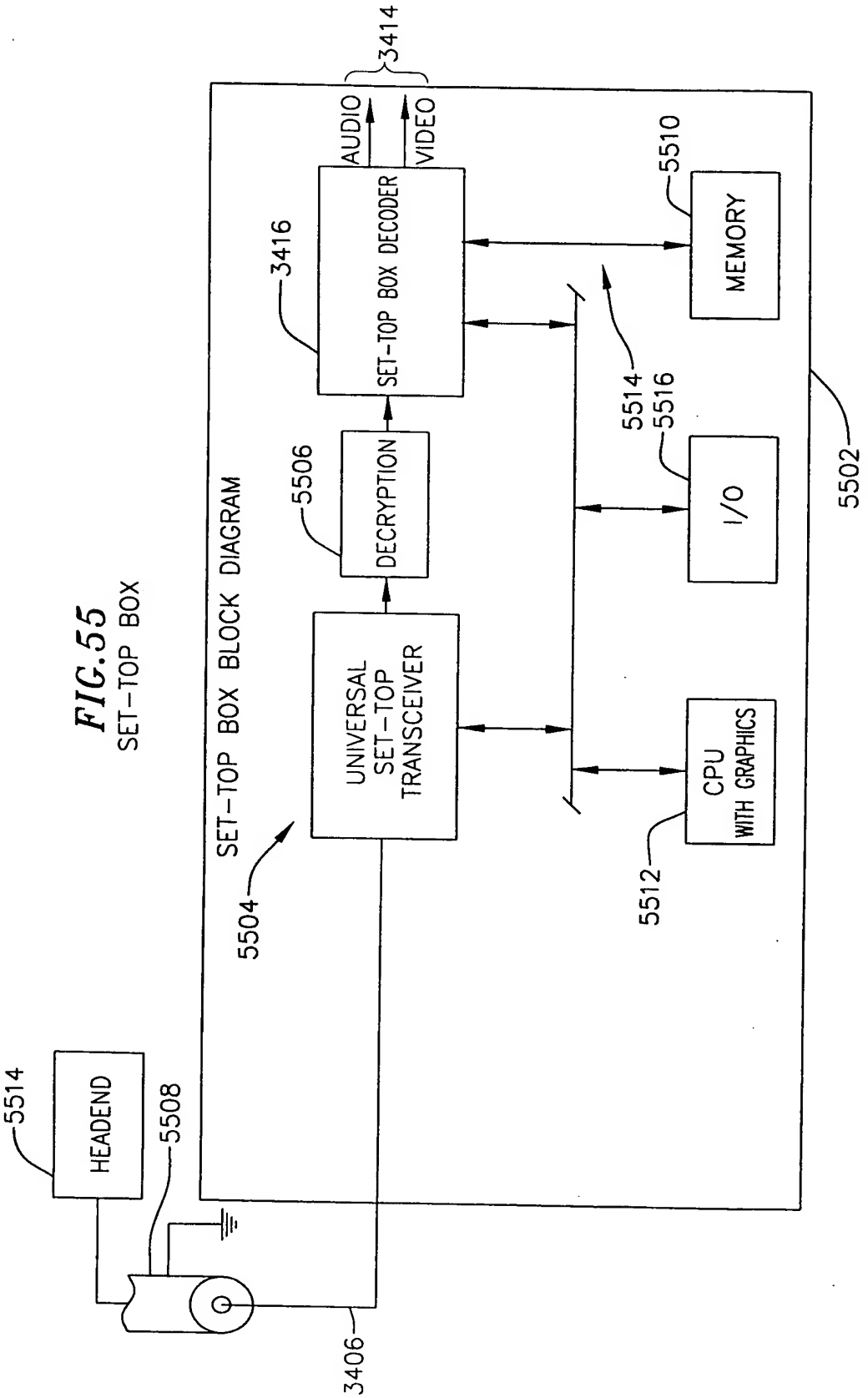


FIG.55
SET-TOP BOX

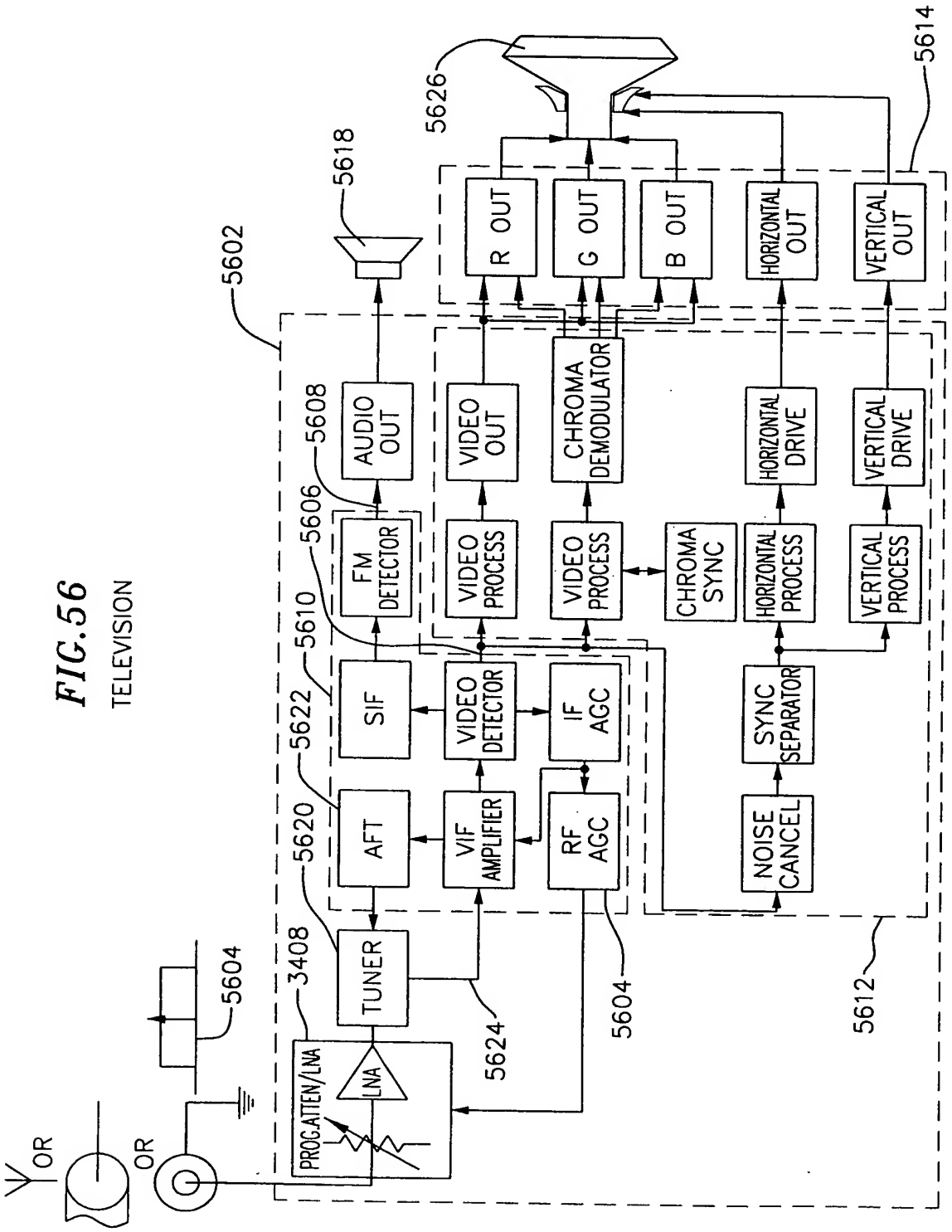
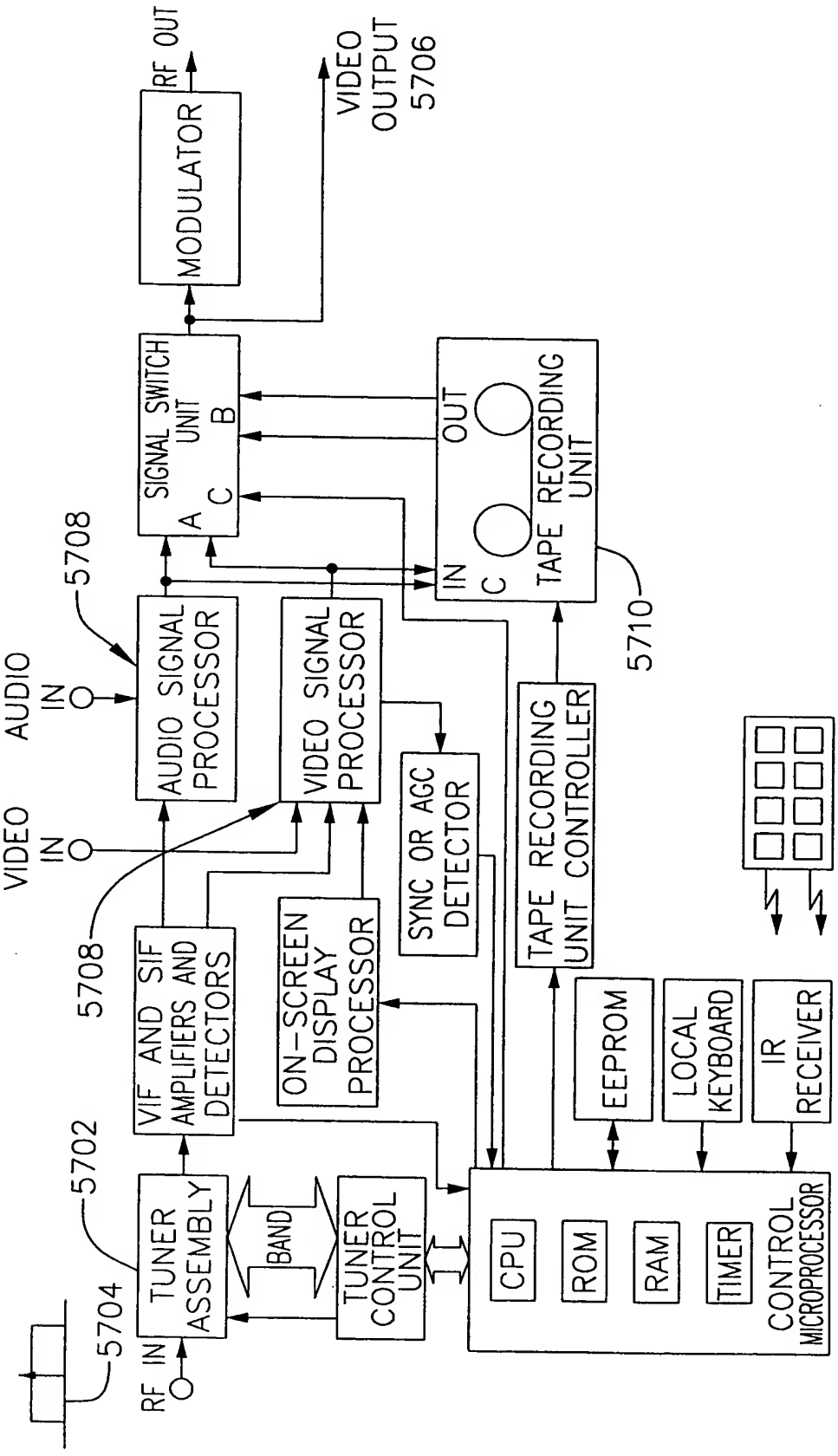

TELEVISION
5602
5604
5606
5608
5610
5612
5614
5618
5620
5622
5624
5626
3408
TUNER
AFT
SIF
FM DETECTOR
AUDIO OUT
VIF AMPLIFIER
VIDEO DETECTOR
VIDEO OUT
RF AGC
IF AGC
VIDEO PROCESS
CHROMA DEMODULATOR
CHROMA SYNC
R OUT
G OUT
B OUT
NOISE CANCEL
SYNC SEPARATOR
HORIZONTAL DRIVE
HORIZONTAL PROCESS
HORIZONTAL OUT
VERTICAL DRIVE
VERTICAL PROCESS
VERTICAL OUT
PROG.ATTEN/LNA
LNA
OR
OR

FIG.56

FIG.57
VCR BLOCK DIAGRAM



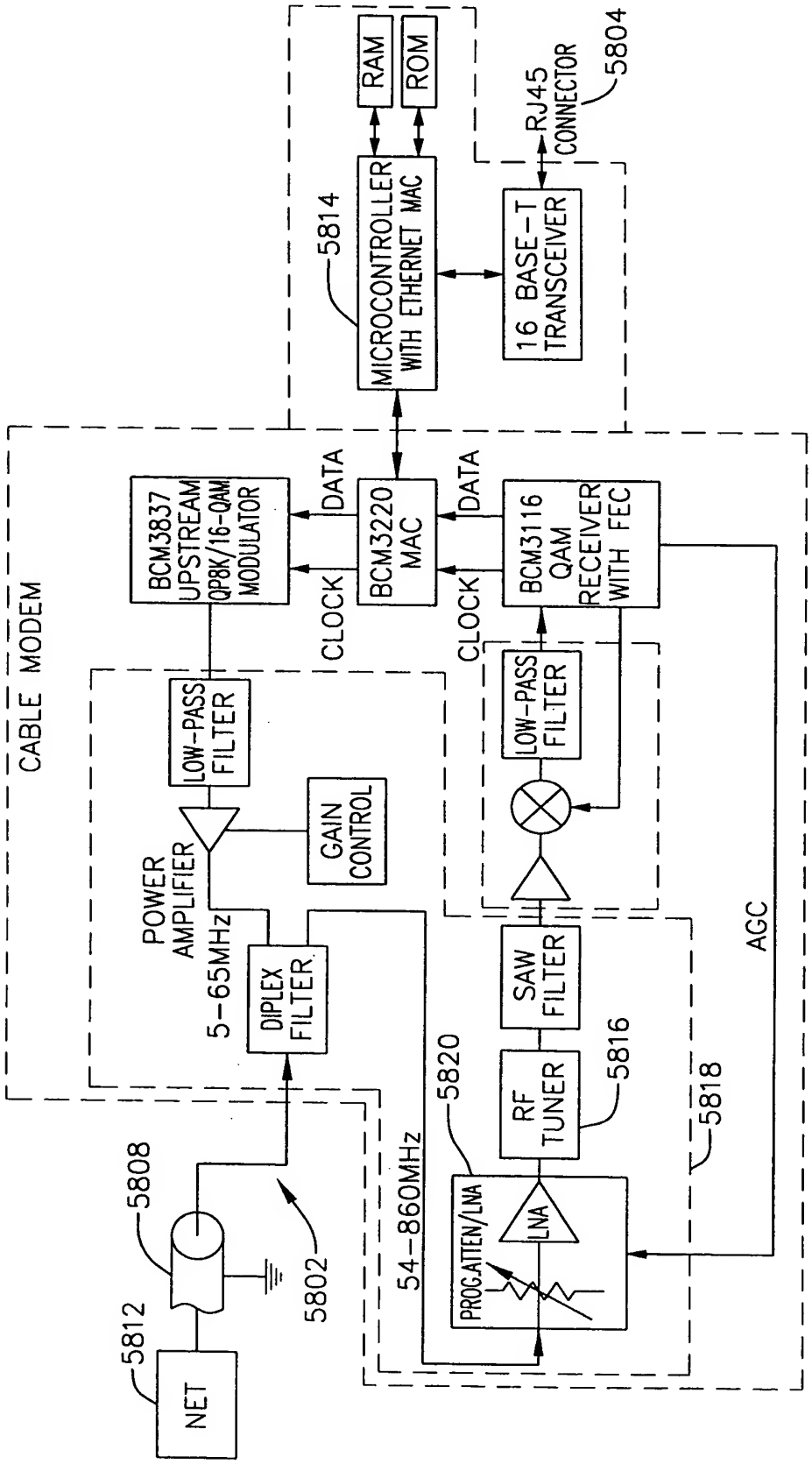

CABLE MODEM
RAM
ROM
RJ45 CONNECTOR
5804
5814
MICROCONTROLLER WITH ETHERNET MAC
16 BASE-T TRANSCEIVER
BCM3837 UPSTREAM QPSK/16-QAM MODULATOR
DATA
BCM3220 MAC
DATA
BCM3116 QAM RECEIVER WITH FEC
CLOCK
CLOCK
LOW-PASS FILTER
LOW-PASS FILTER
GAIN CONTROL
POWER AMPLIFIER
5-65MHz
DIPLEX FILTER
SAW FILTER
RF TUNER
5816
5820
5818
AGC
54-860MHz
PROG.ATTEN/LNA
LNA
5808
5802
5812
NET

FIG.58